

WRDC-TR-89-2040

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TURBINE BLADE  
DATA ACQUISITION SYSTEM  
TECHNICAL REFERENCE

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University of Dayton Research Institute  
Electronic and Computer Development Laboratory  
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Dayton, OH 45469-0001

May 1989

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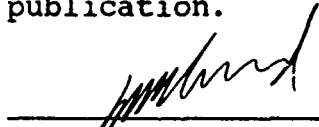
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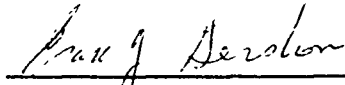
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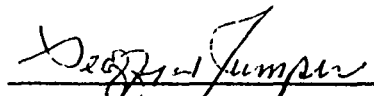
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This report provides design and technical documentation on the Turbine Blade Data Acquisition System developed by the Electronic and Computer Development Laboratory, within the University of Dayton Research Institute. It was designed and fabricated as an analytical tool for structural testing and research on turbine components as part of the Noncontacting Stress Measurement System. This research effort was performed for the Aerospace Mechanics Group of the Research Institute. Michael Drake was the Principal Investigator and Robert Dominic was the Research Engineer in charge of daily activities for this project.

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Documentation . . . . .	Michael Gutman Steve Fuchs
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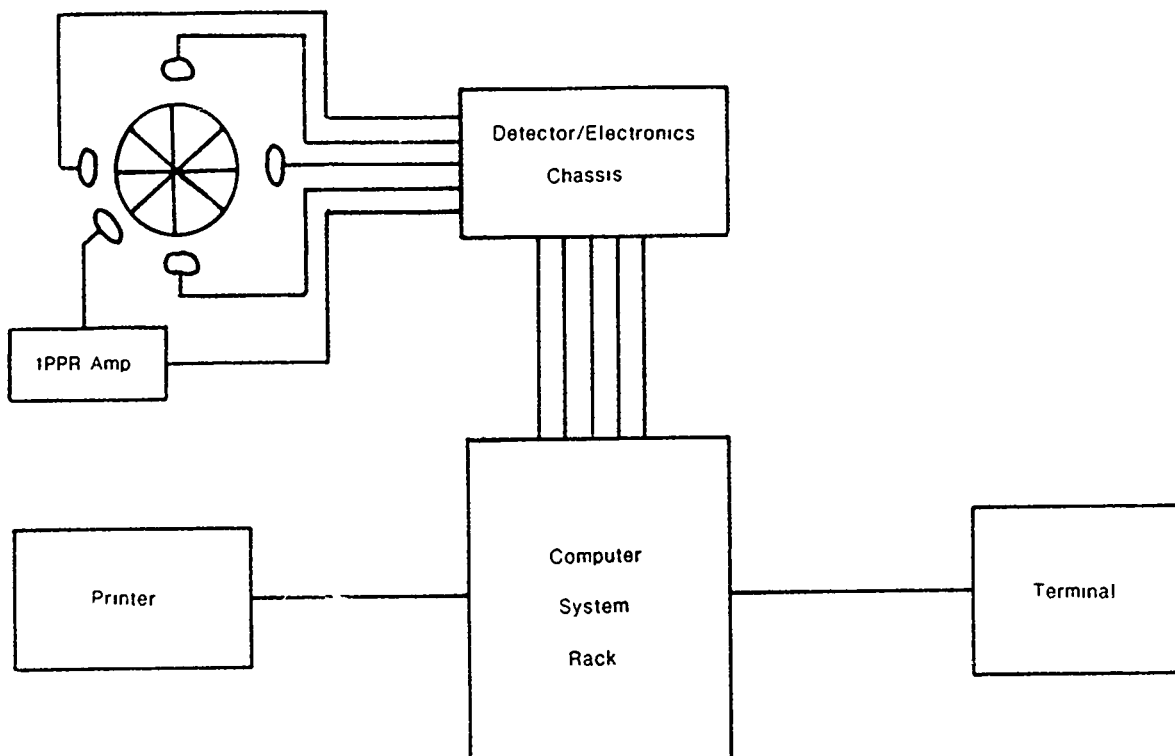


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TITLE TBDAS BLOCK DIAGRAM				FILENAME BLANK PLT	
				FILEDATE 07-Jul-1989	
FIGURE 1	SHEET 1 of 1	DESIGNER ECD	DRAWN BY MJG	FILETIME 07 49 06	
UDRI University of Dayton Research Institute <small>Electronic &amp; Computer Development Laboratory</small>					
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Figure 1: TBDAS Block Diagram

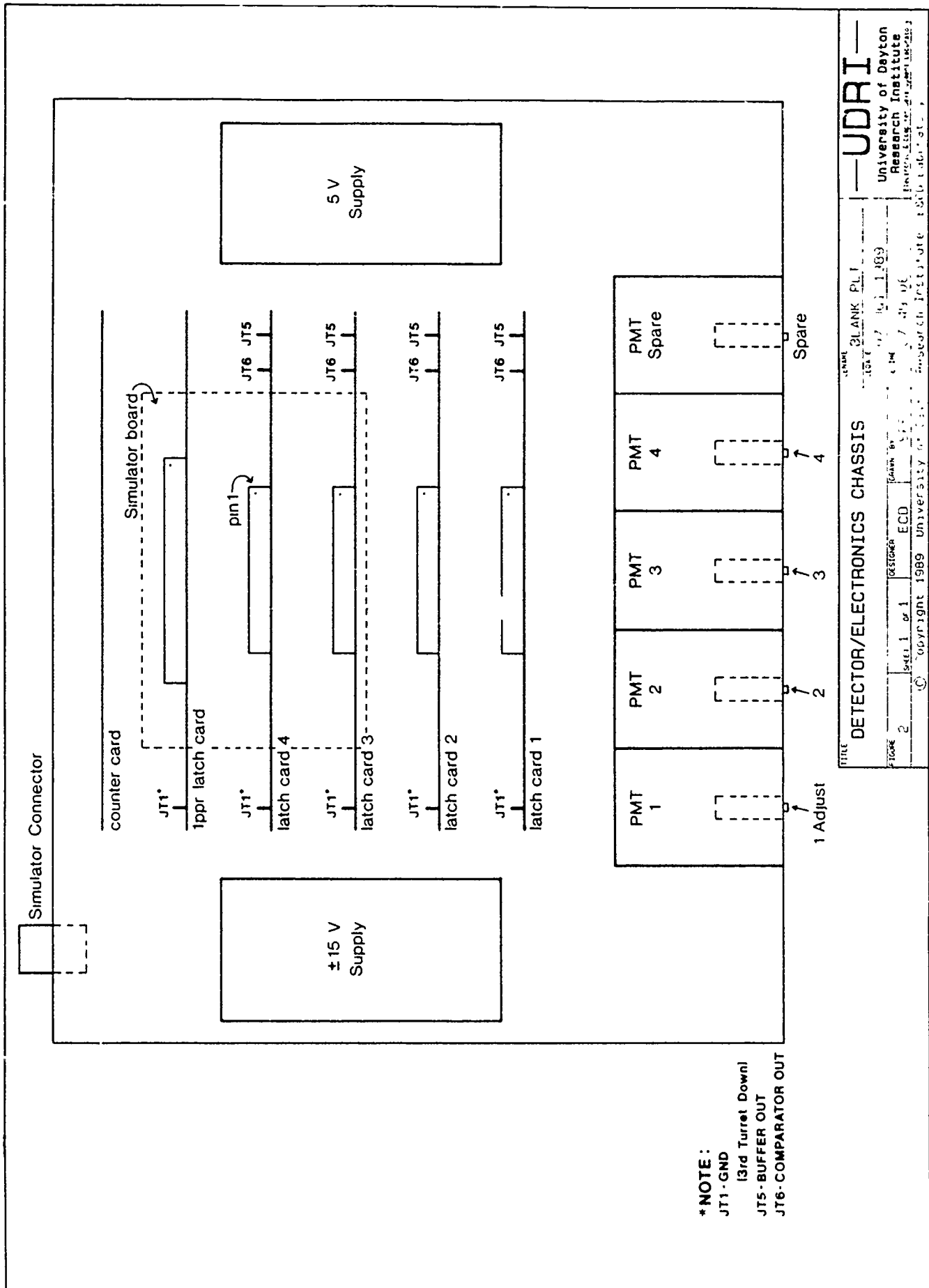


Figure 2: Detector/Electronics Chassis

<b>UDRI</b> University of Dayton Research Institute Dayton, Ohio 45424-0001	
<b>FIGURE 2</b> DETECTOR/ELECTRONICS CHASSIS	<b>BLANK PLT</b> 10/1/89
2 1 of 1 ECD 10/1/89	10/1/89 10/1/89 10/1/89
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# NSMS Data Acquisition System

C = Change Date / Time / Specimen Data

D = Discard Data

H = Histogram

P = Real Time Display

S = Start Taking Data

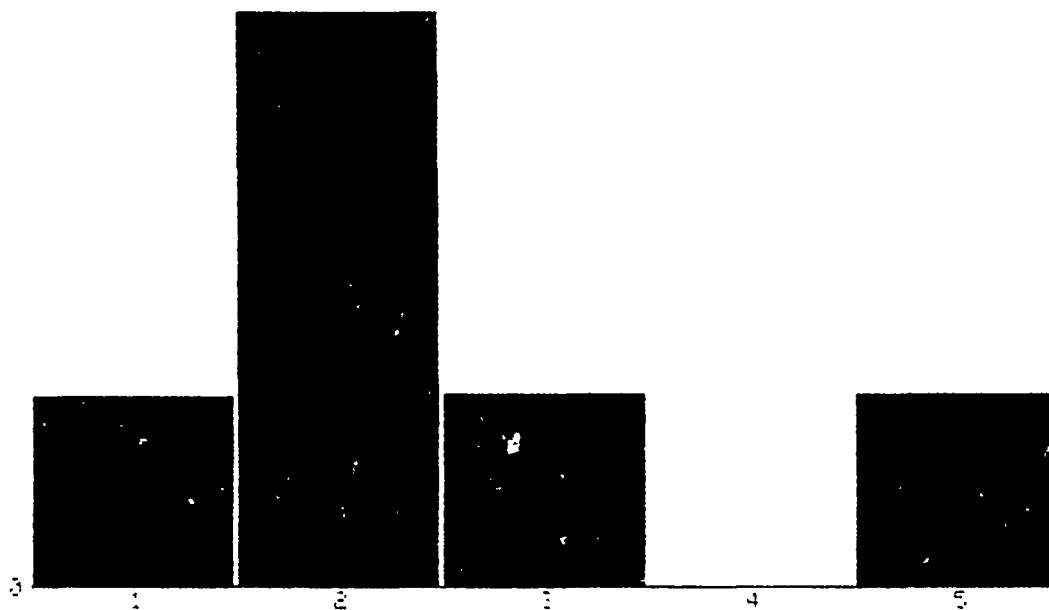
W = Write Data To Tape

TITLE MAIN MENU TERMINAL DISPLAY				FILENAME BLANK PLT		<b>UDRI</b> University of Dayton Research Institute Electronic & Computer Development Laboratory
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FIGURE 3	SHEET 1 of 1	DESIGNER	DRAWN BY	FILETIME 07 49 06		
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Figure 3: Main Menu Terminal Display

TEST RUN Station-1 625 Hz 625 RPM 13-Oct-87 02:34:40

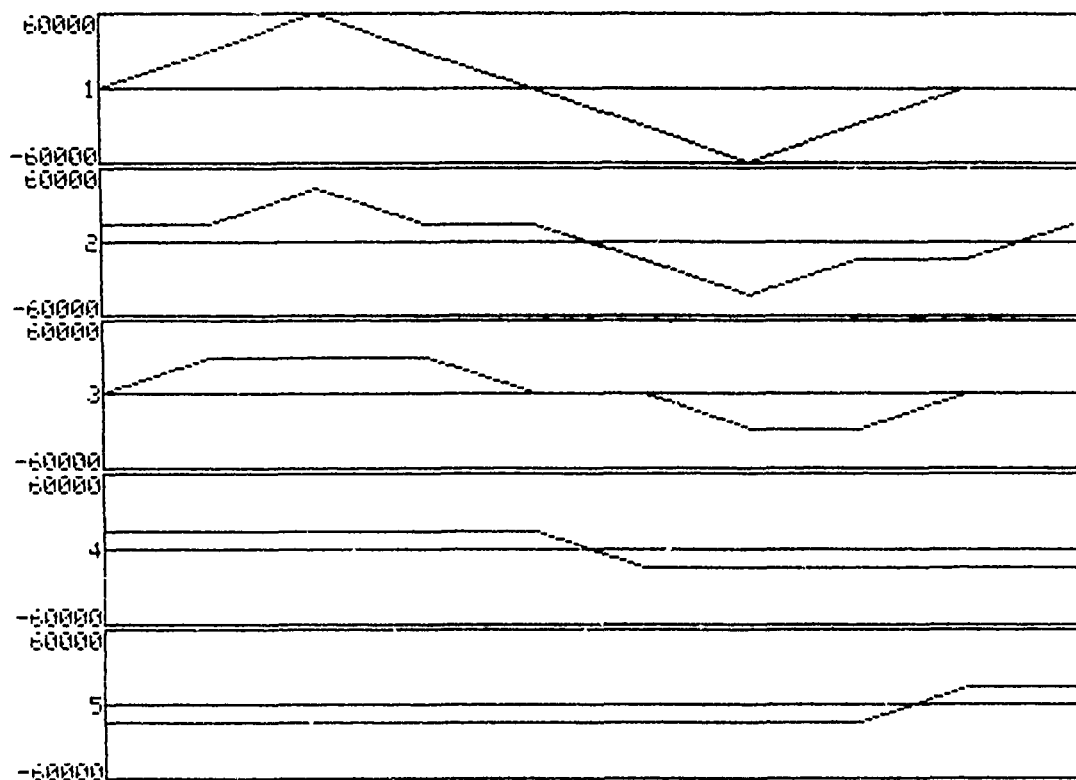
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TITLE HISTOGRAM TERMINAL DISPLAY				FILENAME BLANK.PLT		<b>UDRI</b> University of Dayton Research Institute Electronic & Computer Development Laboratory
				FILEDATE 07-Jul-1989		
FIGURE 4	SHEET 1 of 1	DESIGNER	DRAWN BY	FILETIME 07 49 06		
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Figure 4: Histogram Terminal Display

TEST RUN Station-1 625 Hz 625 RPM 13-Oct-87 08:36:56



TITLE REAL TIME TERMINAL DISPLAY				FILENAME BLANK PLT		<b>UDRI</b> University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE 5				FILEDATE 07-Jul-1989		
SHEET 1 of 1		DESIGNER	DRAWN BY	FILETIME 07 49 06		
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Figure 5: Real Time Terminal Display

# MSMS Data Acquisition System

Revolution 204 of 1000

	Current	Minimum	Maximum
	-----	-----	-----
Speed :	625	625	625 RPM

C = Change Date Time / Specimen Data

D = Discard Data

H = Histogram

P = Real Time Display

S = Start Taking Data

W = Write Data To Tape

TITLE MAIN MENU RUN TIME TERMINAL DISPLAY		FILENAME BLANK FILE		<b>UDRI</b> University of Dayton Research Institute <small>Electronic &amp; Computer Development Laboratory</small>
FIGURE 6		DATE 17-JUL-1989		
SHEET 1 of 1		DESIGNER		FILETIME 07:49:06
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Figure 6: Main Menu Run Time Terminal Display

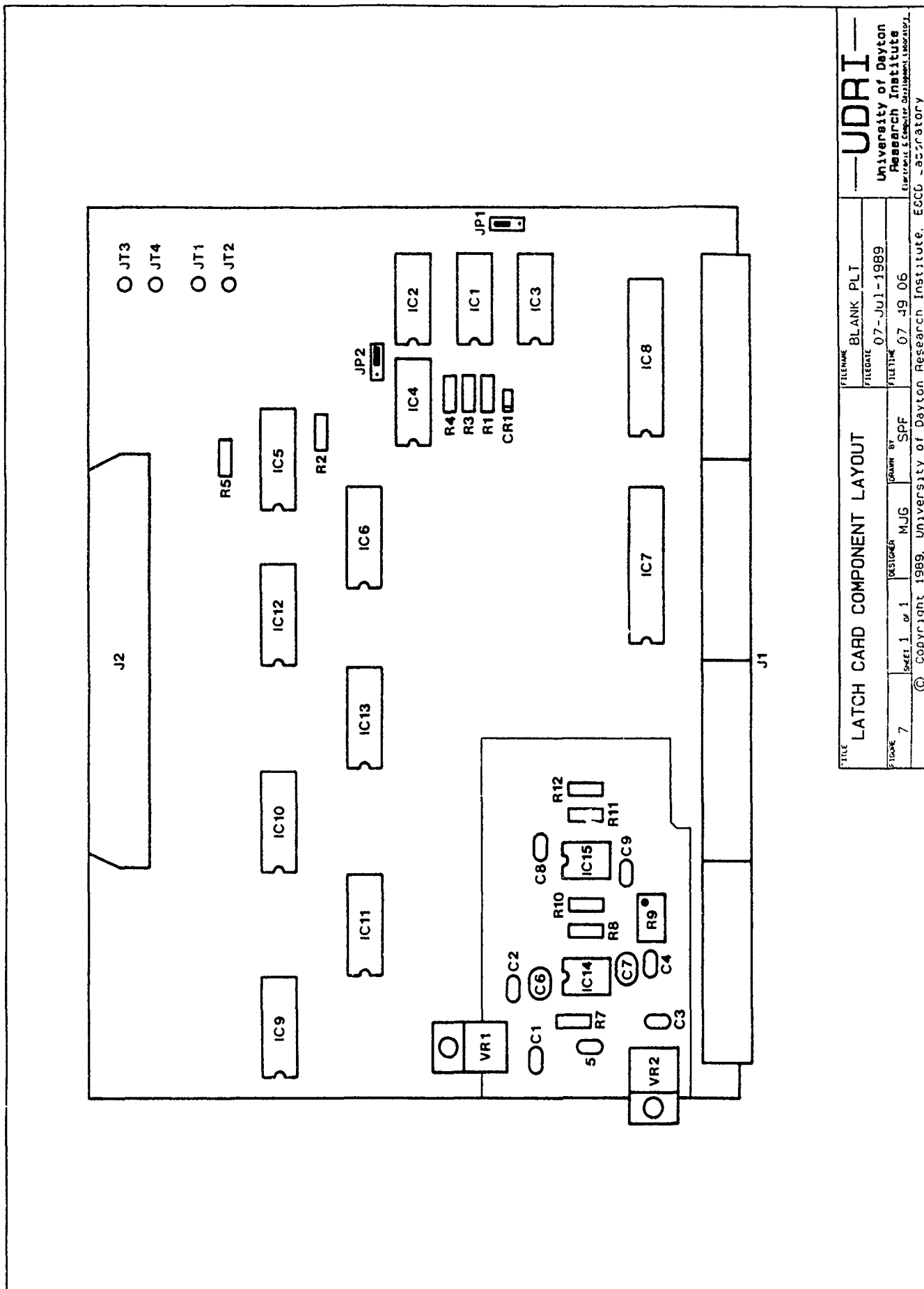
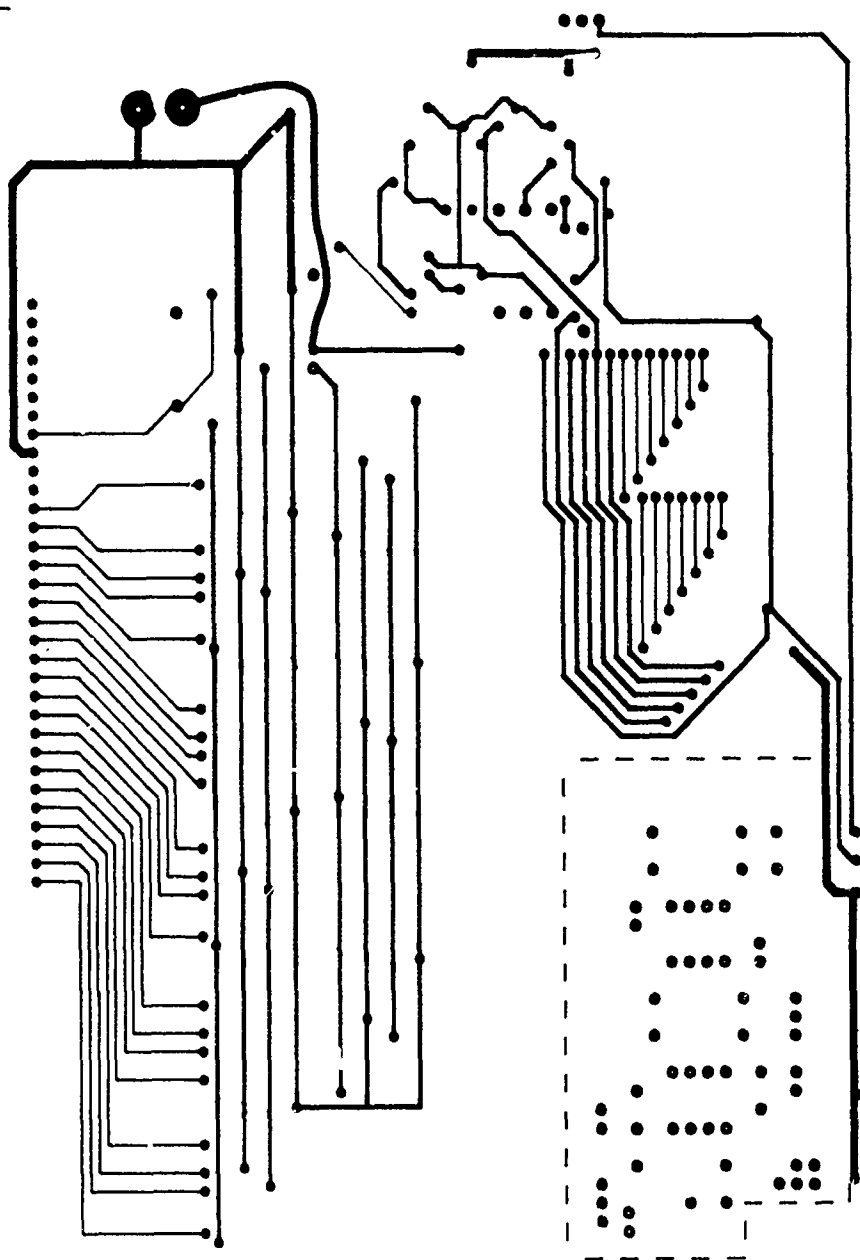
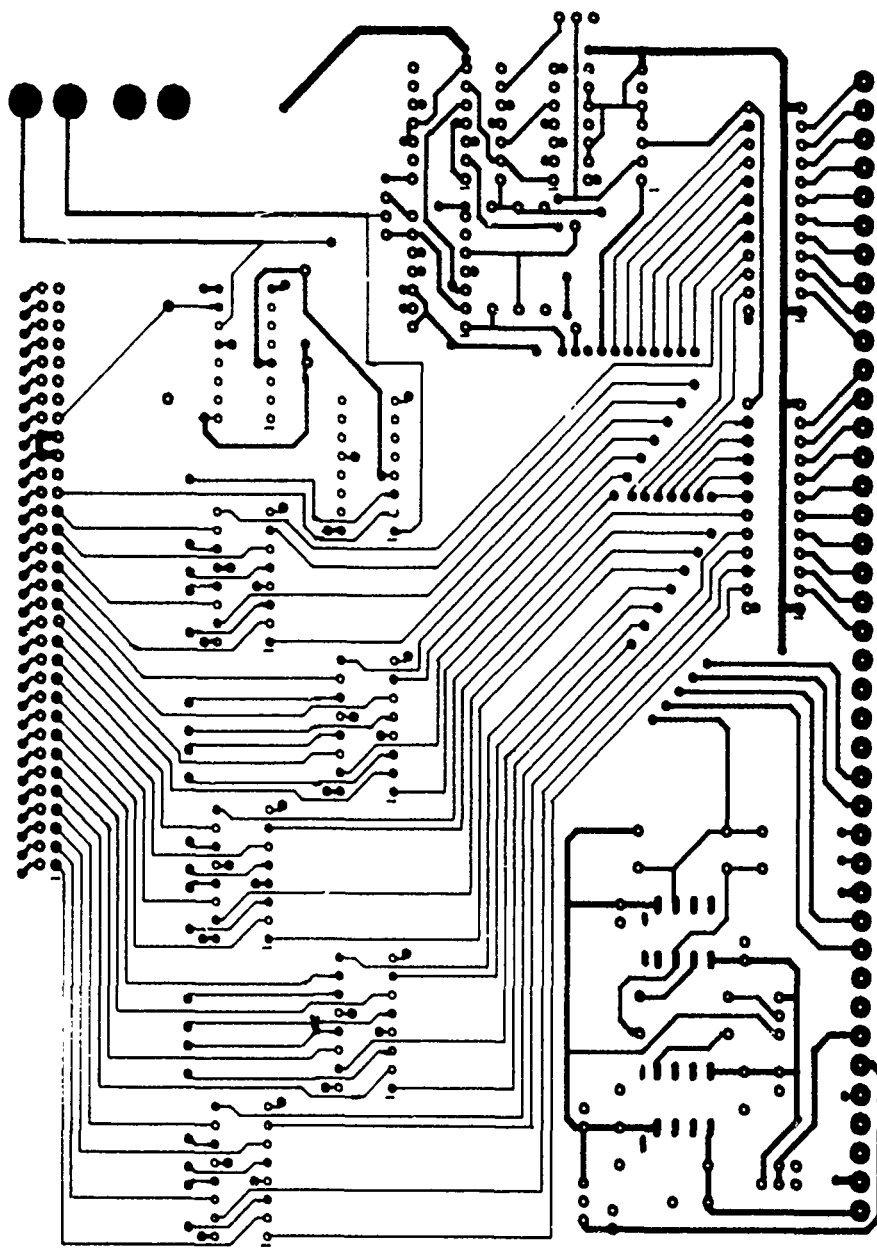


Figure 7: Latch Card Component Layout



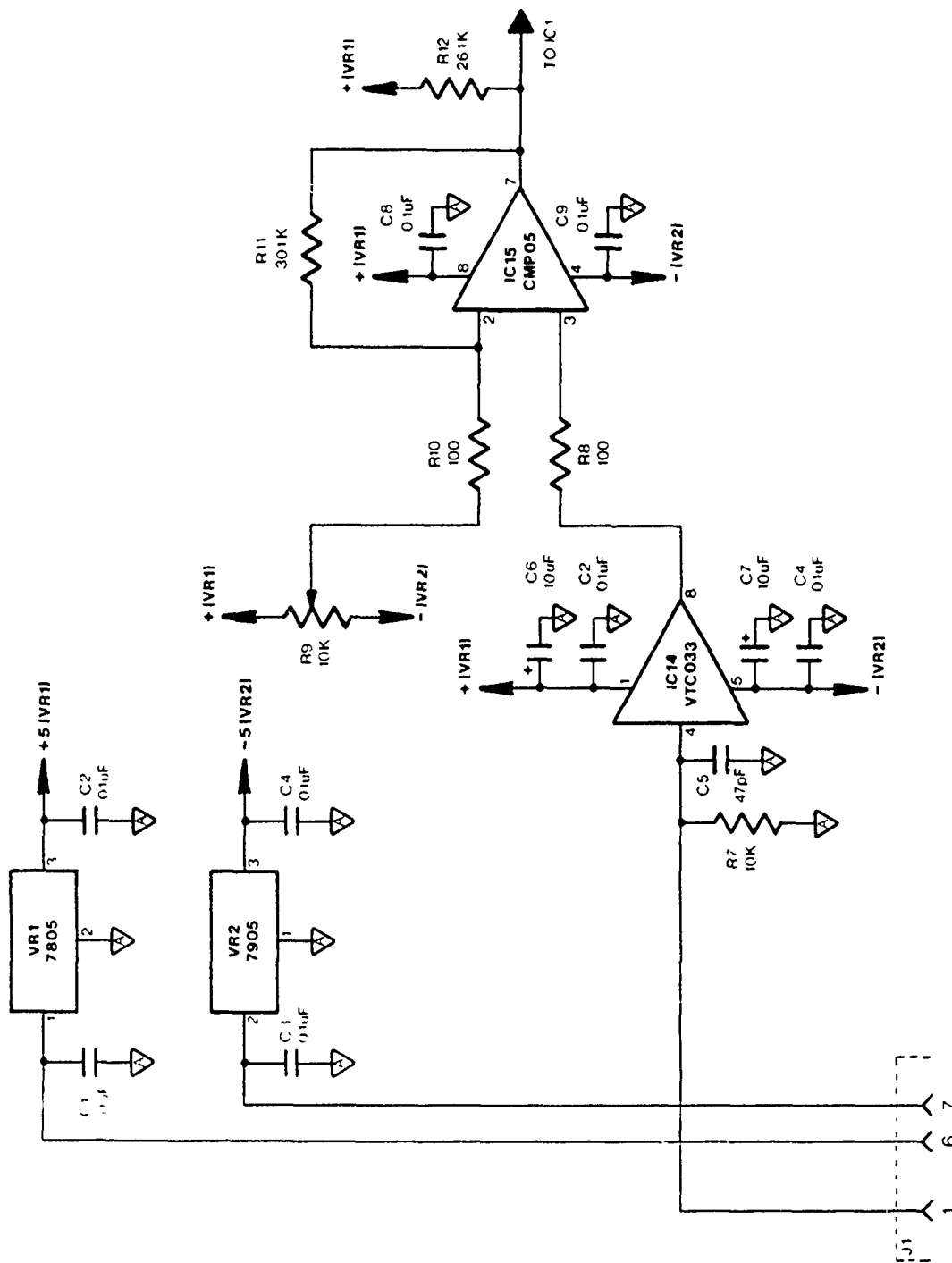
TITLE		LATCH CARD ARTWORK (COMPONENT SIDE)		FILENAME	BLANK PL1	UDRI	
FIGURE		8	SHEET 1 of 1	DESIGNER	MJG	DATE	07-Jul-1988
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Figure 8: Latch Card Artwork (Component Side)



TITLE		LATCH CARD ARTWORK (SOLDER SIDE)		FILENAME BLANK PLI		UDRI	
FIGURE 9	SHEET 1 of 1	DESIGNER MJG	DRAWN BY	FILEDATE	University of Dayton		
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				FILETIME	Electronic & Computer Development Laboratory		
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Figure 9: Latch Card Artwork (Solder Side)



FILETIME				—UDRI—			
LATCH CARD SCHEMATIC DIAGRAM				UNIVERSITY OF DAYTON			
(1 OF 3)				RESEARCH INSTITUTE			
FIGURE	10a	SHEET 1 OF 3	DESIGNER	JMA	DRAWN BY	SPF	FILETIME
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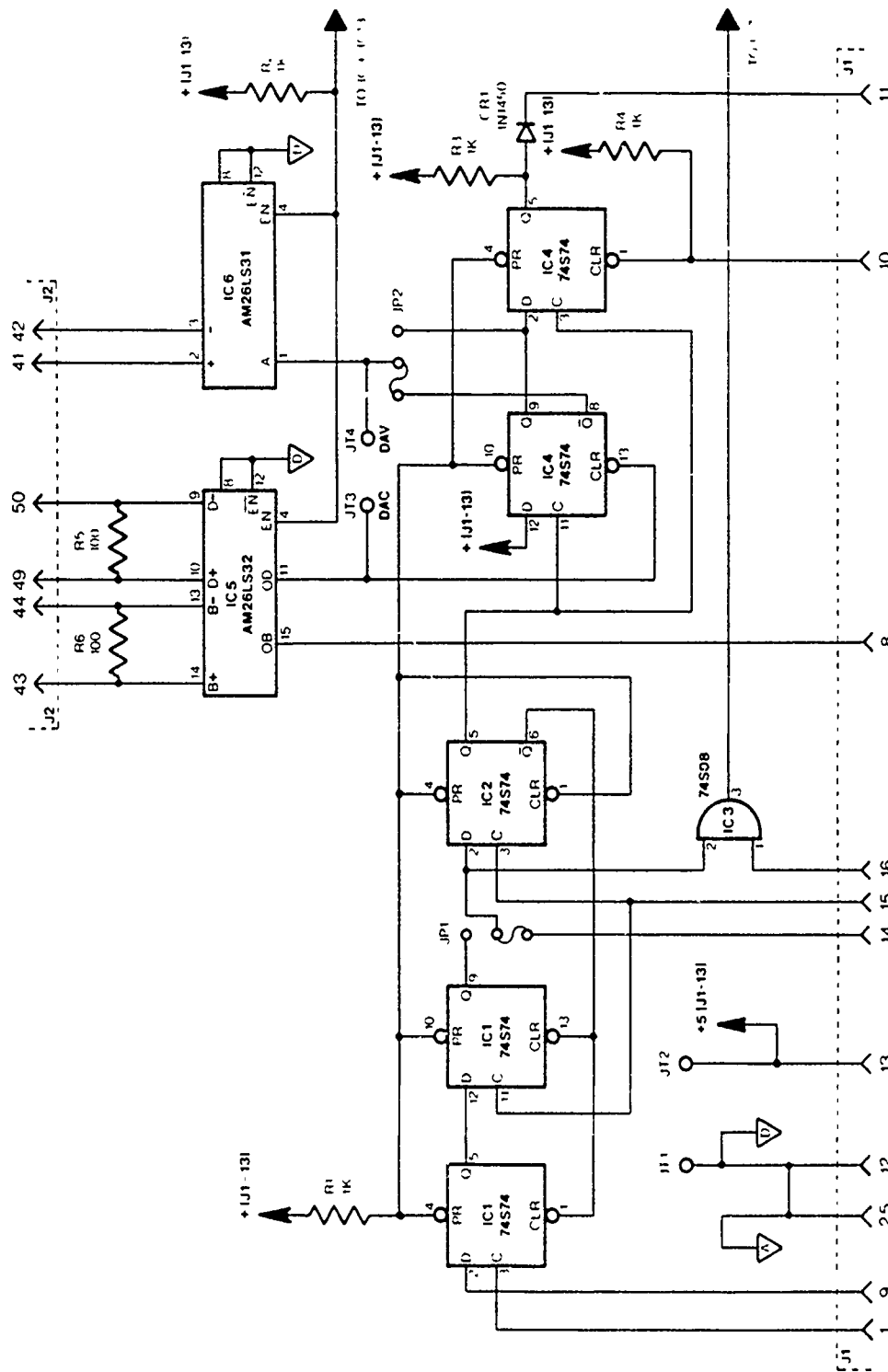


Figure 10b: Latch Card Schematic Diagram (2 of 3)

FILE NAME		BLANK PLT		—UDRI—	
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FILE TIME		07.49.06		Research Institute	
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SHEET 2 OF 3		10b		LATCH CARD SCHEMATIC DIAGRAM	
(2 OF 3)				FIGURE	

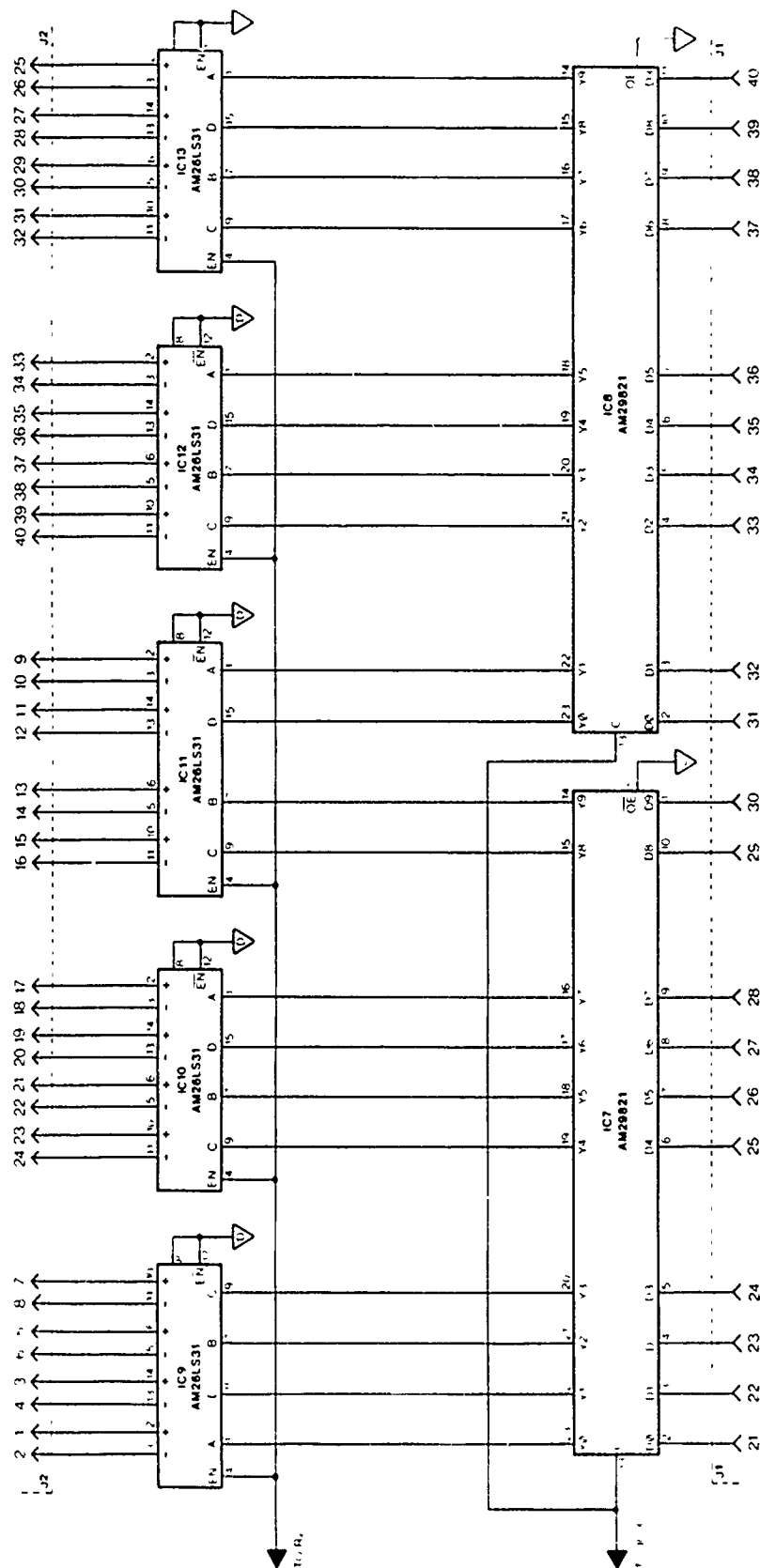
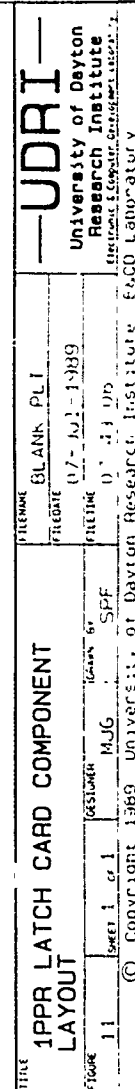


Figure 10c: Latch Card Schematic Diagram (3 of 3)

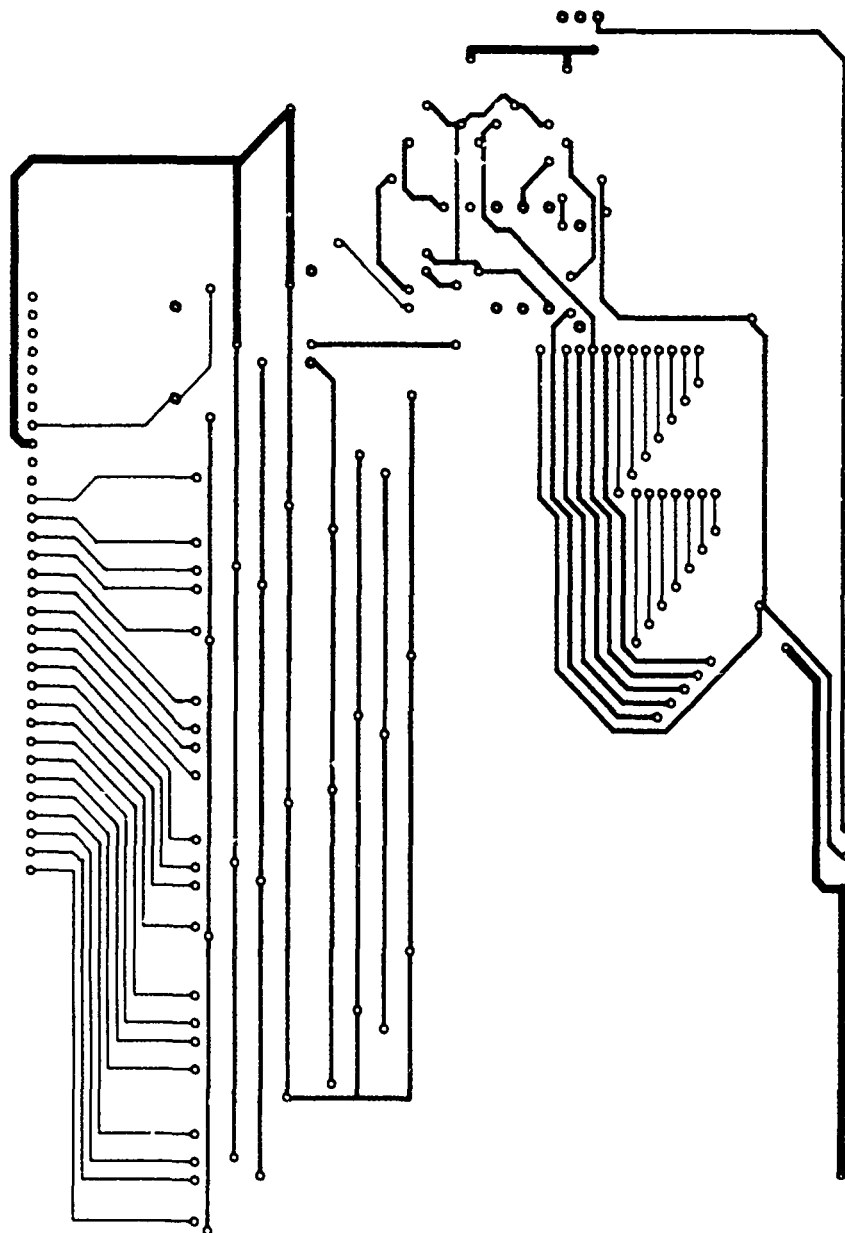
# Latch Card Parts List

Part Number	Description
R1 - R5	1 KOhm
R7 10	KOhm
R8, R10	100 Ohm
R11	30.1 KOhm
R12	26.1 KOhm
R9	10KOhm Trimpot
C1 - C4, C8, C9	0.1 uF
C5	47 pF
C6, C7	10 uF Tantalum
IC1, IC2, IC4	74S74
IC3	74S08
IC5	Am26LS32
IC6, IC9 - IC13	Am26LS31
IC7, IC8	Am29821
IC14	VTC033
IC15	CMP05
VR1	7805
VR2	7905
CR1	1N4150
J1	Molex .156 10 position (x4)
J2	Ansley Blue Macs 50 pin male

Table 1: Latch Card Parts List

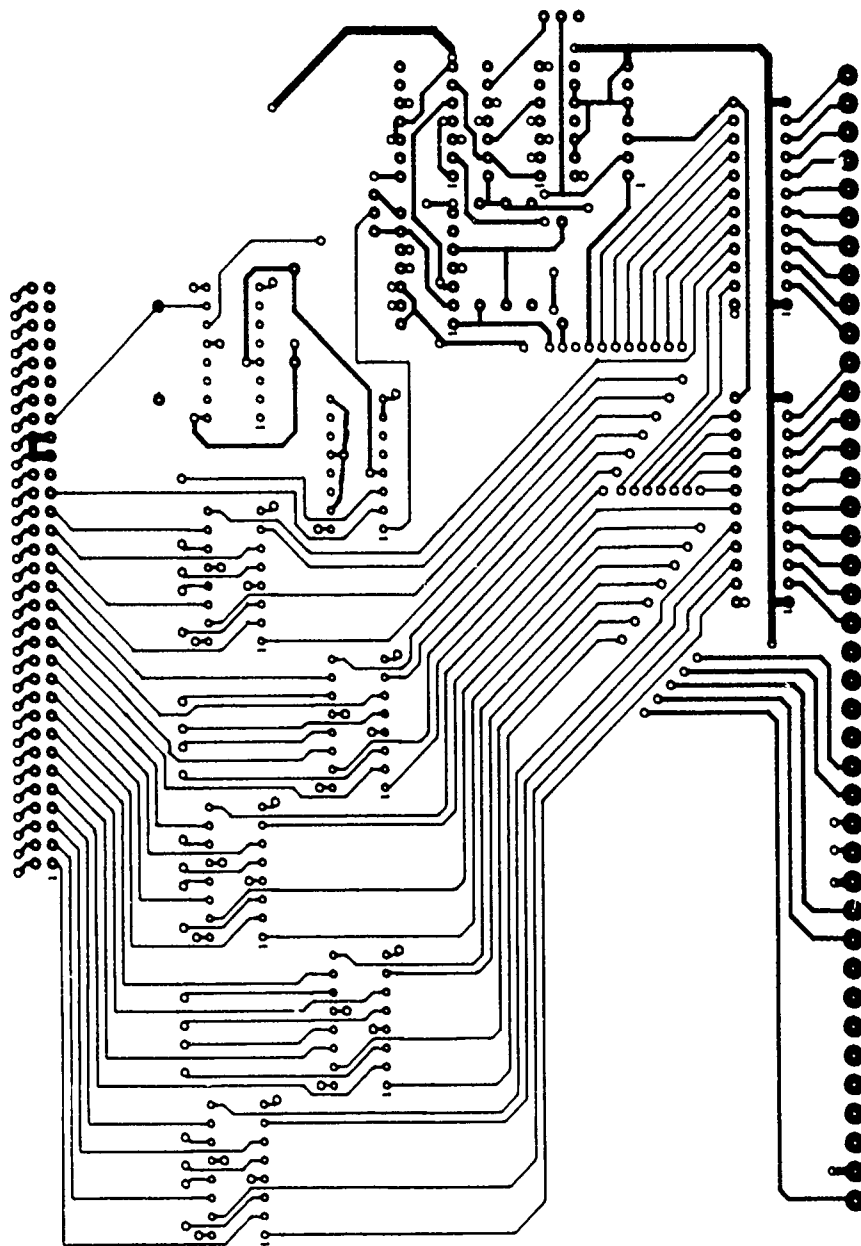


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TITLE				FILENAME		—UDRI—	
1PPR LATCH CARD ARTWORK (COMPONENT SIDE)				BLANK PLT		University of Dayton Research Institute	
FIGURE 12				DATE		07-Jul-1989	
SHEET 1 of 1				DESIGNER		07 49:06	
				DRAWN BY		Electronic & Computer Development Laboratory	
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Figure 12: 1PPR Latch Card Artwork (Component Side)



1PPR LATCH CARD ARTWORK (SOLDER SIDE)				FILENAME: BLANK.PLT		—UDRI—	
FIGURE 13				DATE: 07-01-1989		University of Dayton Research Institute	
SHEET 1 of 1				DESIGNER: MJG		Electronic Computer Development Laboratory	
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Figure 13: 1PPR Latch Card Artwork (Solder Side)

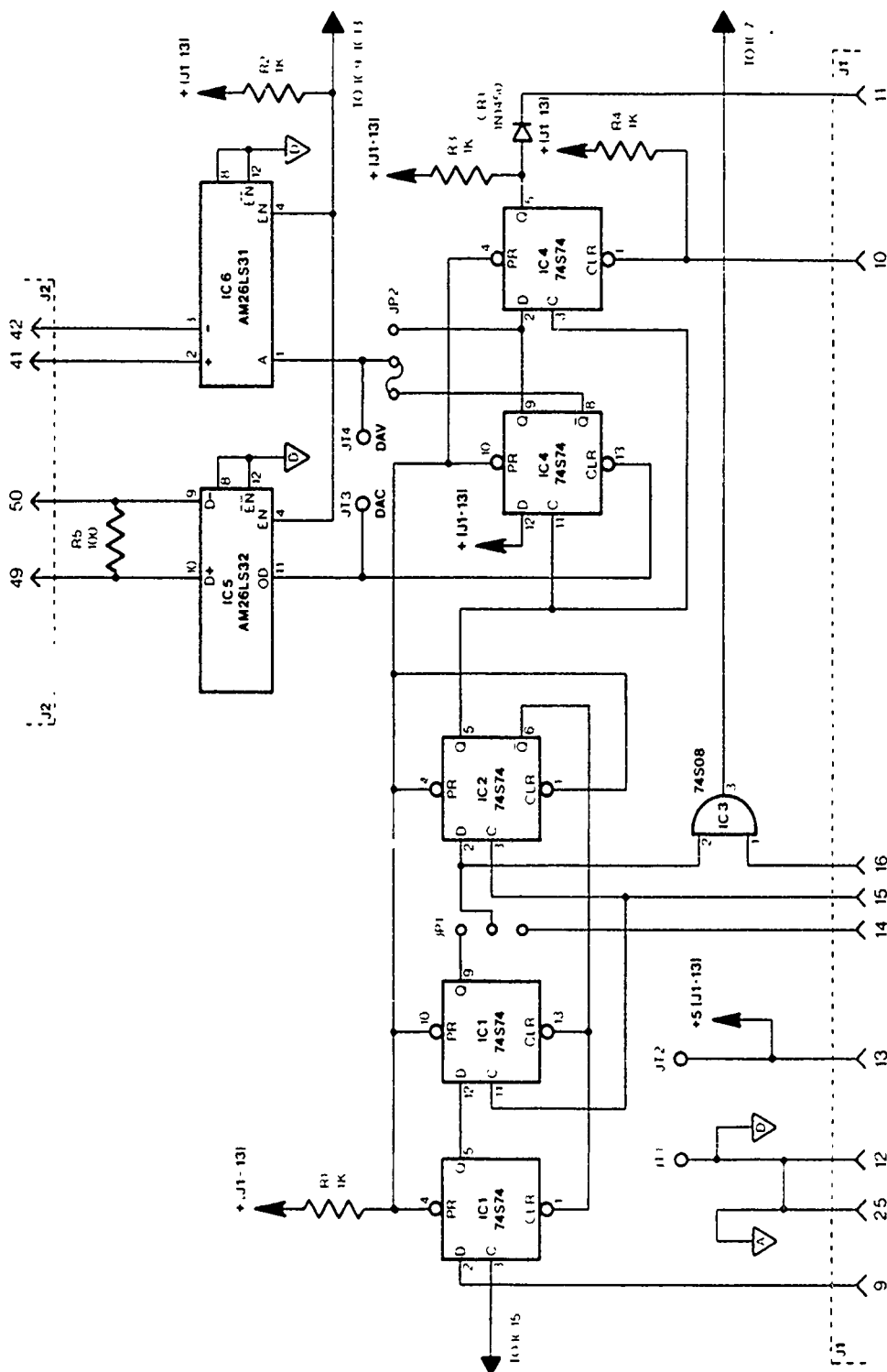


Figure 14a: 1PPR Latch Card Schematic Diagram (1 of 2)

1PPR LATCH CARD SCHEMATIC DIAGRAM (1 OF 2)				UDRI—	
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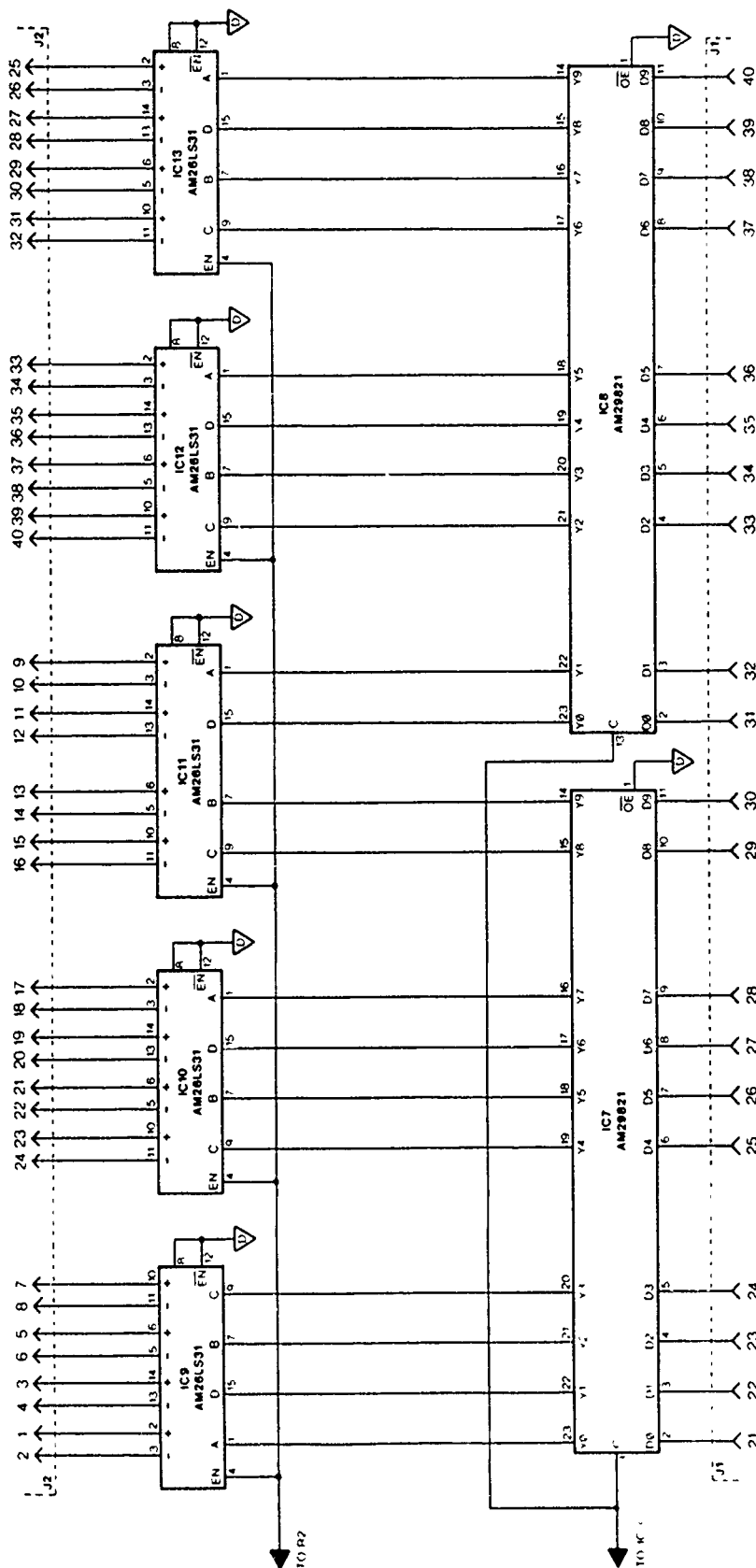


Figure 14b: 1PPR Latch Card Schematic Diagram (2 of 2)

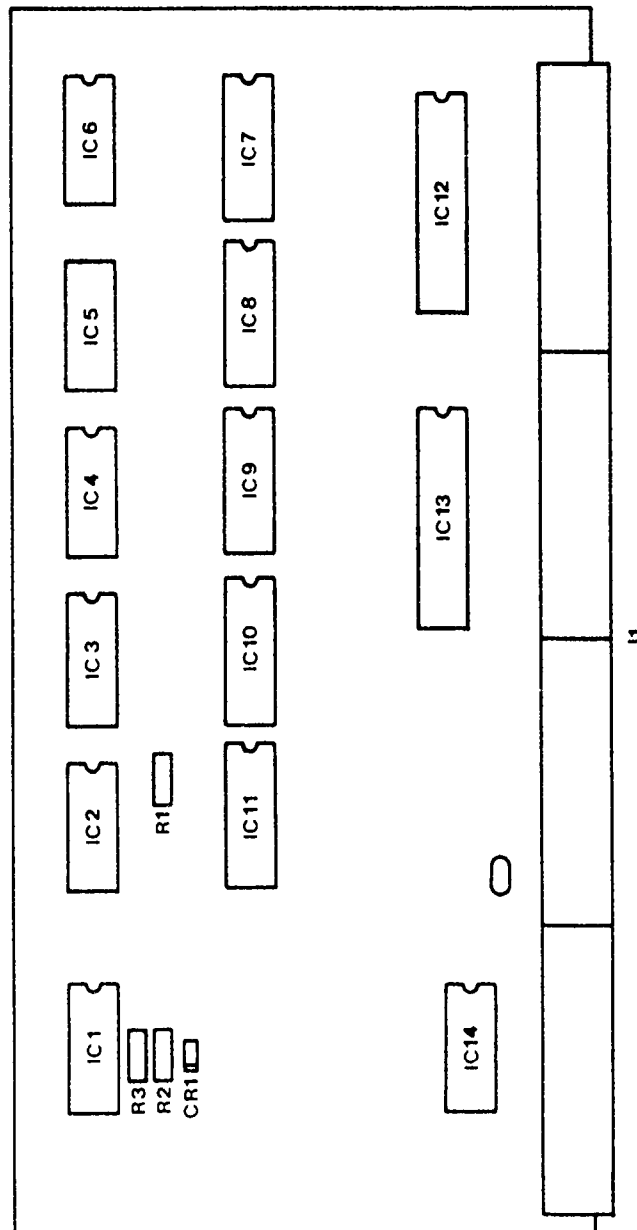
1PPR LATCH CARD SCHEMATIC DIAGRAM (2 OF 2)				FILE NAME	BLANK PLT
FIGURE	14b	SHEET 2 OF 2	DESIGNER	DATE	07-JUL-1989
			JMA	QUANT	07 49 06
© Copyright 1989, University of Dayton Research Institute ESCD Laboratory				FILE NAME	07-JUL-1989
				FILE NAME	07 49 06

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Research Institute  
Electronic & Computer Development Laboratory

# 1PPR Latch Card Parts List

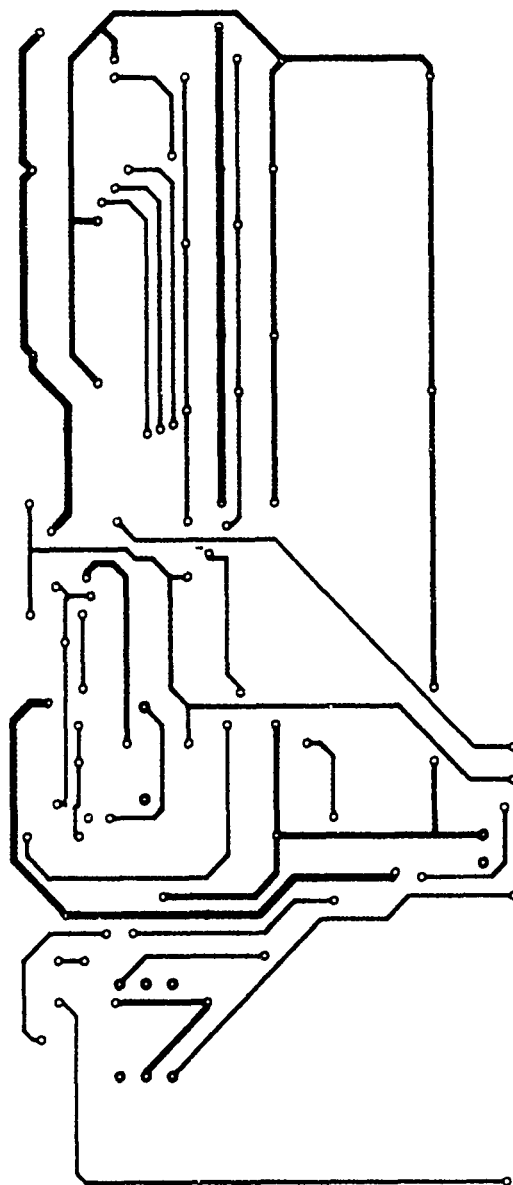
Part Number	Description
R1 - R6	1 KOhm
IC1, IC2, IC4	74S74
IC3	74S08
IC5	Am26LS32
IC6, IC9 - IC13	Am26LS31
IC7, IC8	Am29821
CR1	1N4150
J1	Molex .156 10 position (x4)
J2	Ansley Blue Macs 50 pin male

Table 2: 1PPR Latch Card Parts List



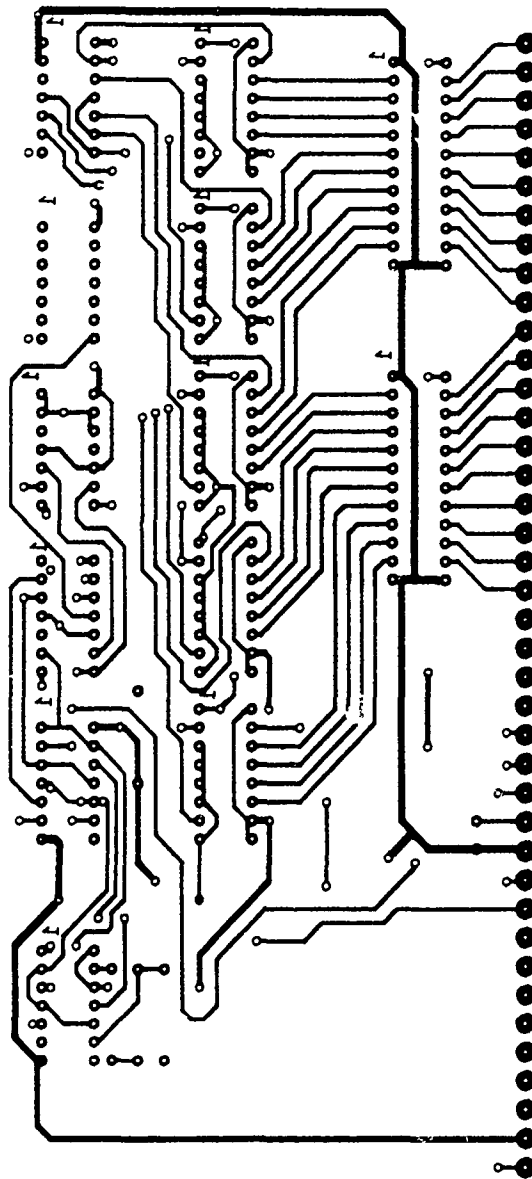
TITLE				COUNTER CARD COMPONENT LAYOUT				FILENAME		BLANK PLT		—UDRI—	
FIGURE : E				SHEET 1 of 1		DESIGNER : M =		DRAWN BY : SPF		DATE : 07-Jul-1989		University of Dayton Research Institute Electronics Development Laboratory	
										FILETIME : 07 49 06		Copyright 1989, University of Dayton Research Institute, EECN Laboratory	

Figure 15: Counter Card Component Layout



TITLE				—UDRI—	
COUNTER CARD ARTWORK (COMPONENT SIDE)				FILENAME	BLANK PLT
FIGURE	16	SHEET 1 of 1	DESIGNER	FILEDATE	07-Jul-1989
				DESIGNED BY	07 49 06
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Figure 16: Counter Card Artwork (Component Side)



TITLE		COUNTER CARD ARTWORK (SOLDER SIDE)		FILENAME	BLANK. PLT	—UDRI—	
FIGURE	17	SHEET 1 of 1	DESIGNER	MUG	DRAWN BY	University of Dayton	
						Research Institute	
						Electronics & Computer Development Laboratory	
						Copyright 1989, University of Dayton Research Institute	
						E800 Laboratory	
						07-49-06	
						07-JUL-1989	

Figure 17: Counter Card Artwork (Solder Side)

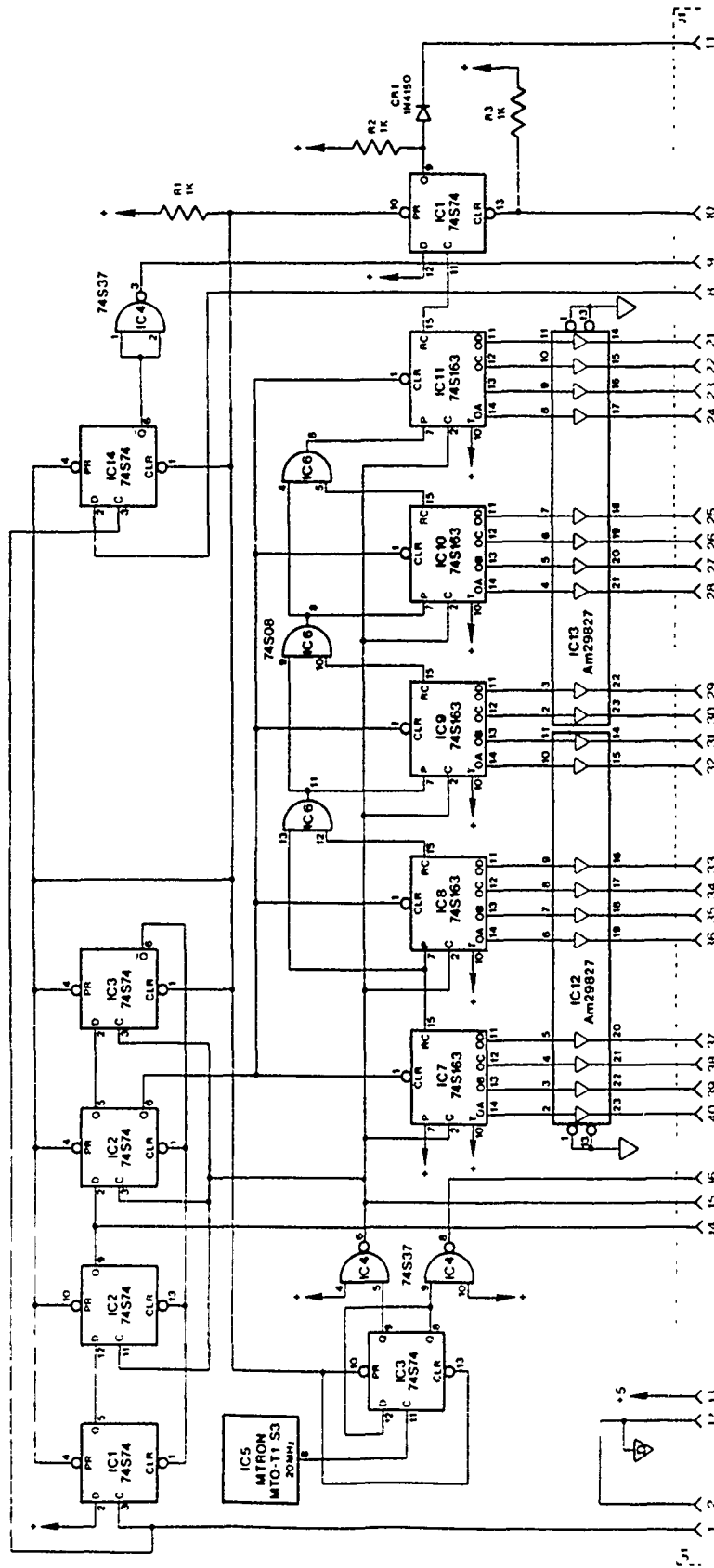


Figure 18: Counter Card Schematic Diagram

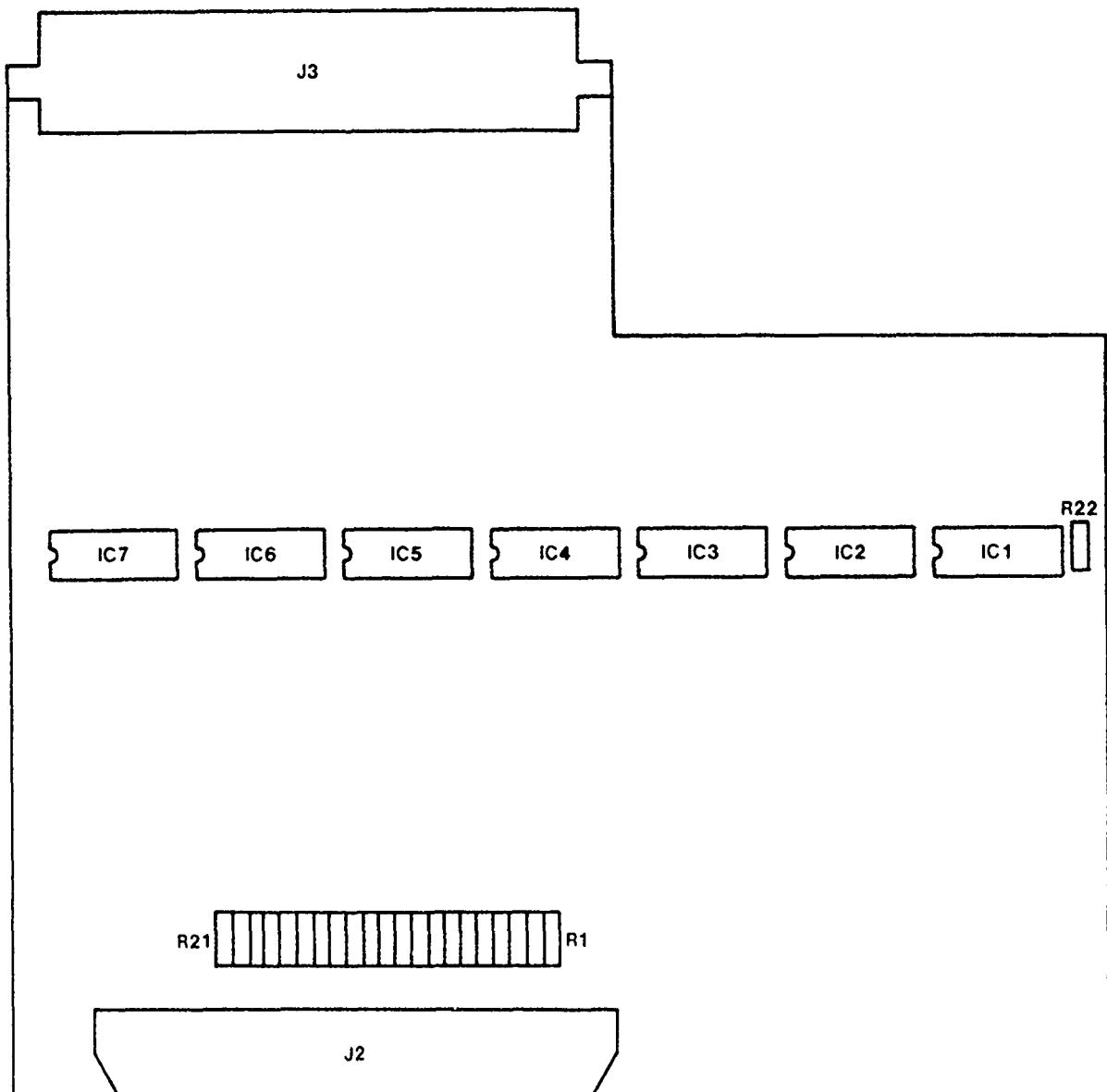
TITLE				COUNTER CARD SCHEMATIC DIAGRAM				FILENAME BLANK PLT				—UDRI— University of Dayton Research Institute <small>(Electronics &amp; Computer Organization Laboratory)</small>							
FIGURE 18				SHEET 1 of 1				DESIGNER JMA				DRAWN BY SPF				FILEDATE 07-Jul-1989			
												FILETIME 07 49.06							
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UDRI  
University of Dayton  
Research Institute  
Electronic & Computer Development Laboratory

#### Counter Card Parts List

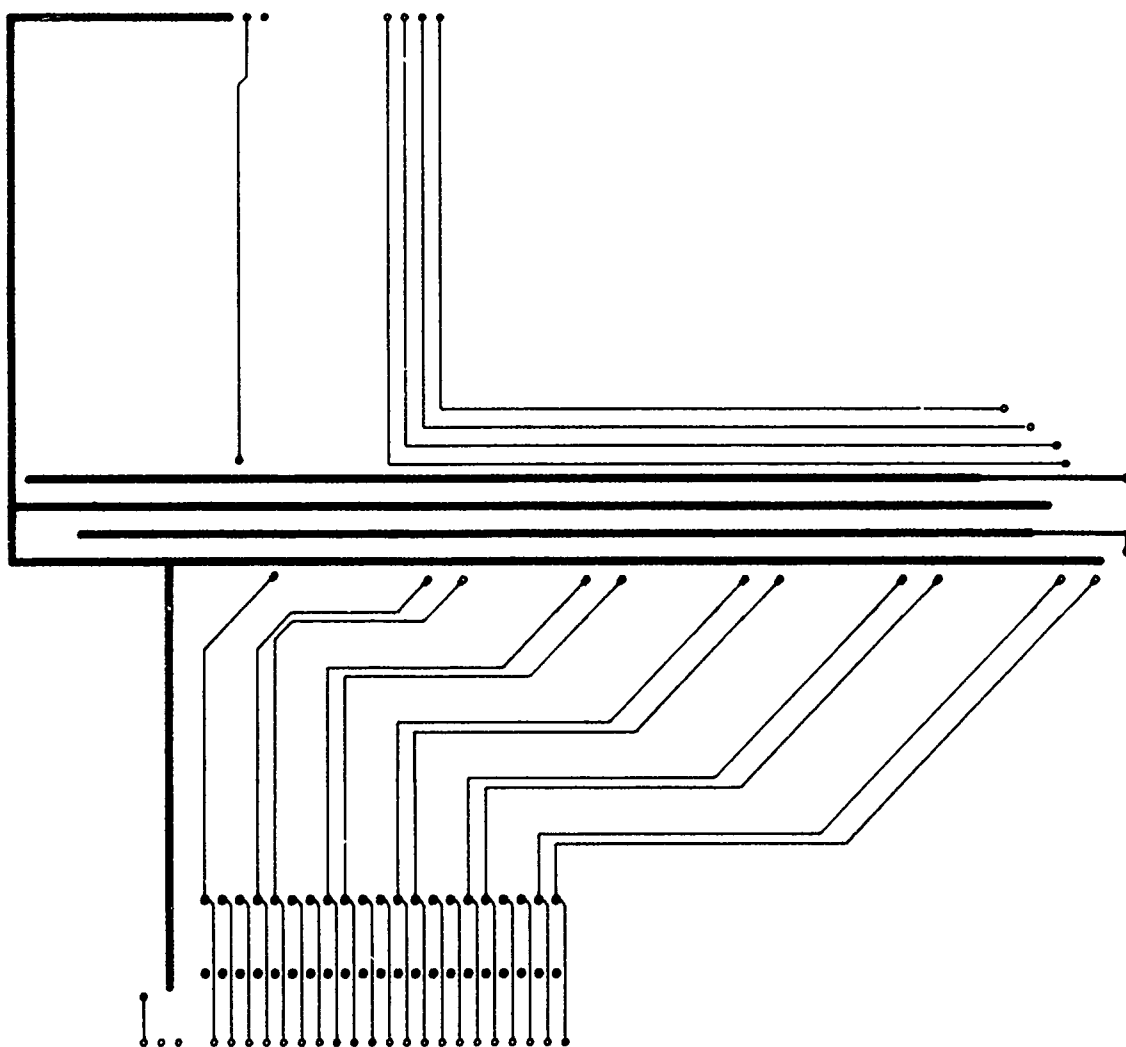
Part Number	Description
R1 - R3	1 KOhm
IC1 - IC3	74S74
IC4	74S37
IC5	MT0-T1-S3 (Mtron)
IC6	74S08
IC7 - IC11	74S163
IC12, IC13	A-29827
CR1	1N4150
J1	Molex .156 10 position (x4)

Table 3: Counter Card Parts List



<b>RECEIVER AND 1PPR RECEIVER CARDS COMPONENT LAYOUT</b>				FILENAME: BLANK PLT		<b>UDRI</b> University of Dayton Research Institute <small>Electronic &amp; Computer Development Laboratory</small>
FIGURE 19				FILEDATE: 07-Jul-1989		
SHEET 1 of 1		DESIGNER: MJG	DRAWN BY: SPF	FILETIME: 07 49 06		
© Copyright 1989, University of Dayton Research Institute ESCD Laboratory						

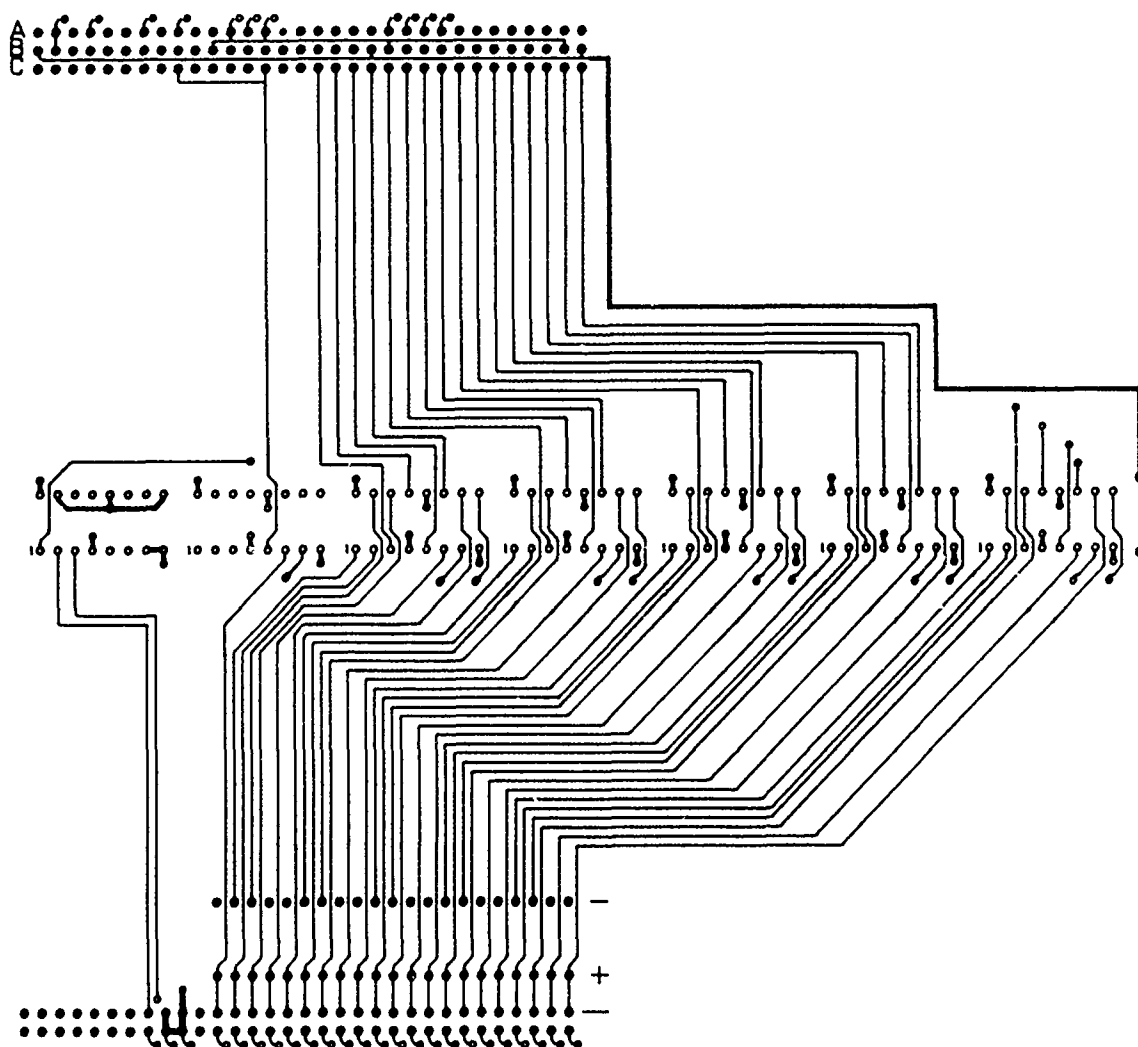
Figure 19: Receiver and 1PPR Receiver Cards Component Layout



<b>TITLE</b> RECEIVER AND 1PPR RECEIVER CARDS ARTWORK (COMP. SIDE)				<b>FILENAME</b> BLANK.PLT	<b>UDRI</b> University of Dayton Research Institute Electronic & Computer Development Laboratory
<b>FIGURE</b> 20	<b>SHEET</b> 1 of 1	<b>DESIGNER</b> MJG	<b>DRAWN BY</b> B	<b>CREATED</b> 07 Jul 1989	
				<b>FILETIME</b> 07 49 06	

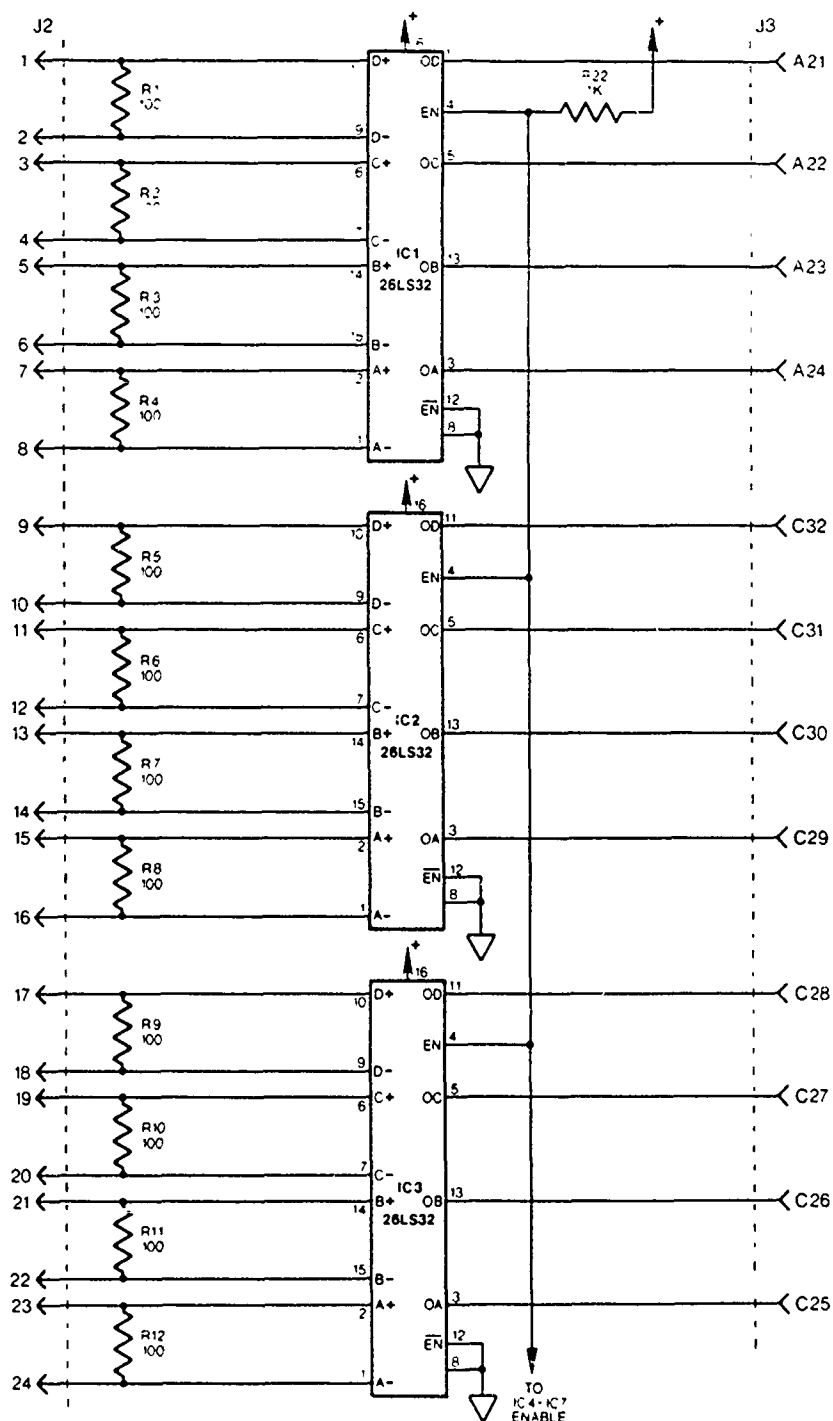
© Copyright 1989 University of Dayton Research Institute, ESCD Laboratory

Figure 20: Reciever and 1PPR Receiver Cards Artwork (Comp. Side)



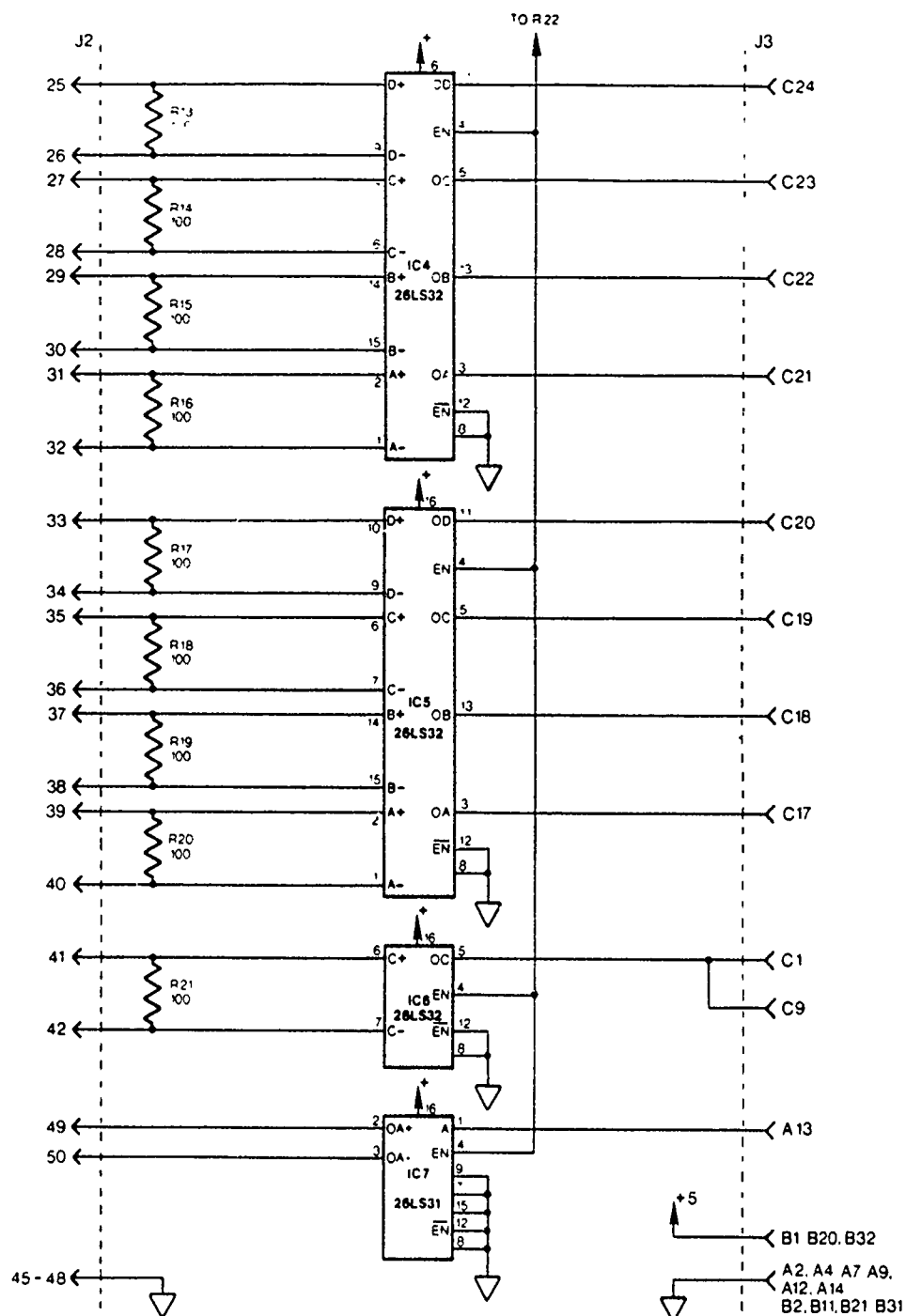
TITLE RECEIVER AND 1PPR RECEIVER CARDS ARTWORK (SOLDER SIDE)				FILENAME BIANK PLT	<div>UDRI</div> <div>University of Dayton Research Institute</div> <div>Electronic &amp; Computer Development Laboratory</div>
FIGURE 21				FILEDATE 07-Jul-1989	
SHEET 1 of 1				FILETIME 07 49 06	
DESIGNER MJG				DRAWN BY	
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Figure 21: Receiver and 1PPR Receiver Cards Artwork (Solder Side)



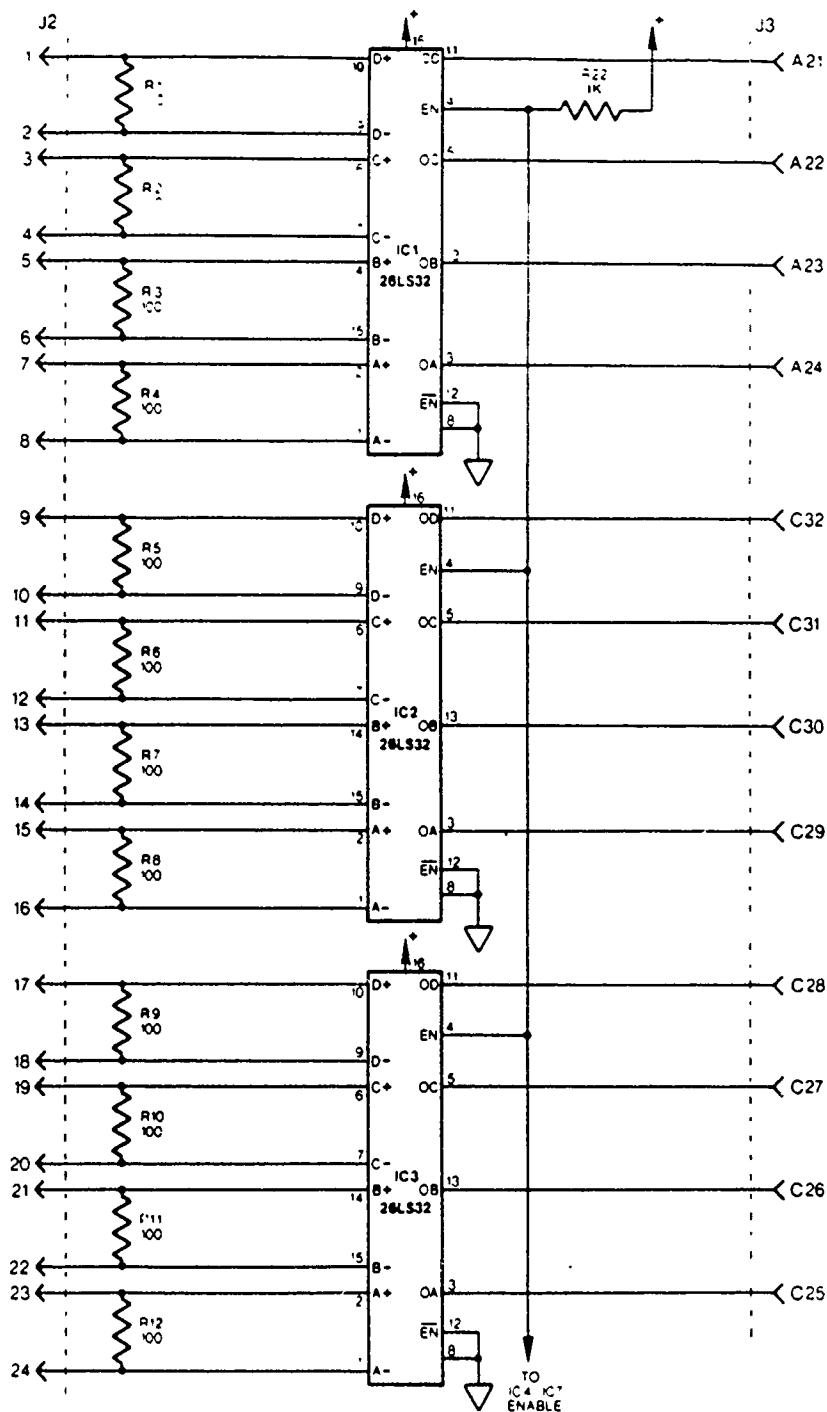
<b>TITLE</b> RECEIVER CARD SCHEMATIC DIAGRAM (1 OF 2)				<b>FILENAME</b> BLANK.PLT		<b>UDRI</b> University of Dayton Research Institute Electronic & Computer Development Laboratory	
<b>FIGURE</b> 22a				<b>FILEDATE</b> 07 Jul 1989			
<b>SHEET 1 of 2</b>				<b>FILETIME</b> 07 49 06			
<b>DESIGNER</b> JMA				<b>DRAWN BY</b> SPF		© Copyright 1989 University of Dayton Research Institute EGCD Laboratory	

Figure 22a: Receiver Card Schematic Diagram (1 of 2)



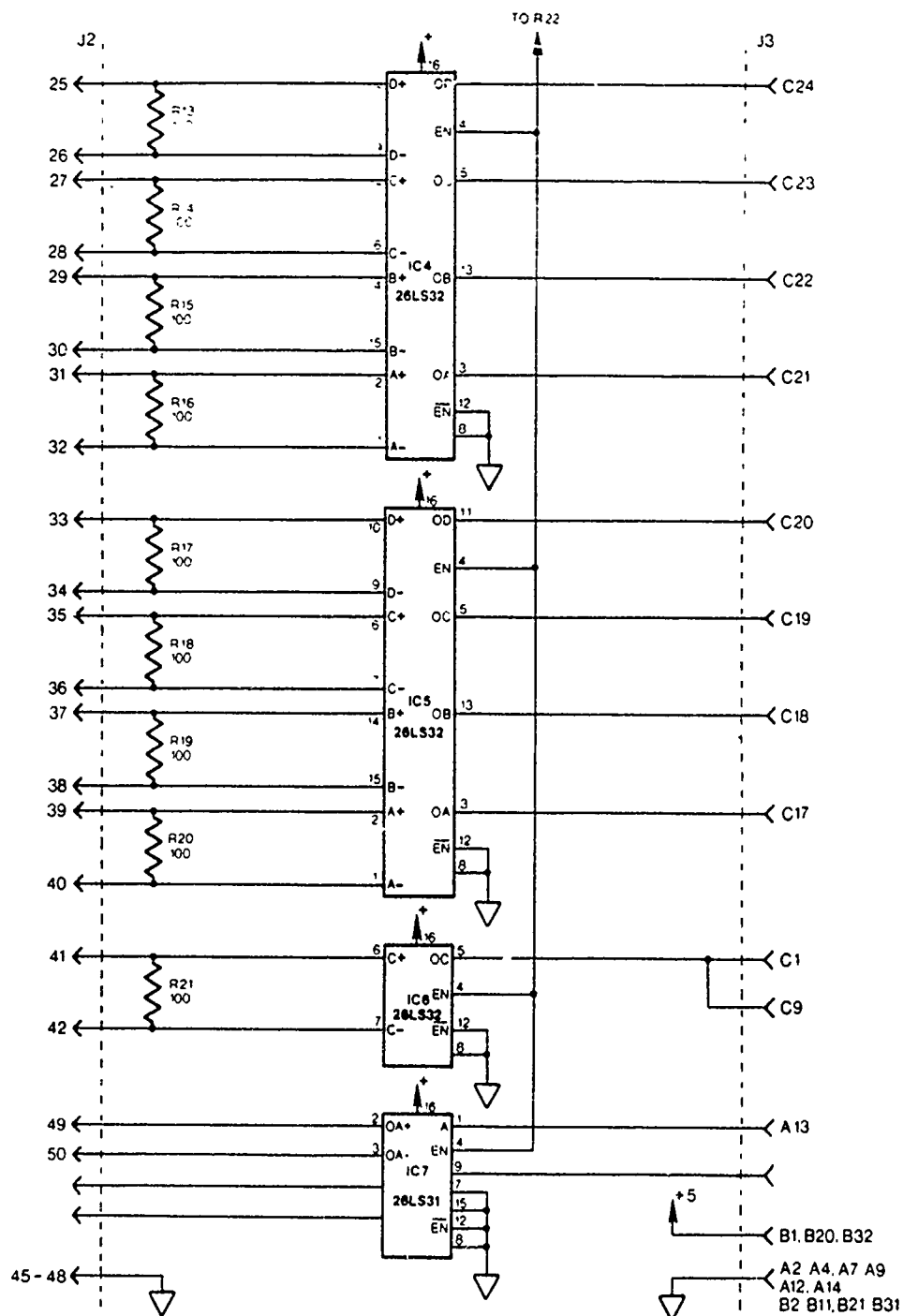
TITLE RECEIVER CARD SCHEMATIC DIAGRAM (2 OF 2)				FILENAME BLANK PLT		<b>UDRI</b> University of Dayton Research Institute <small>Electronic &amp; Computer Development Laboratory</small>
				FILEDATE 07-Jul-1989		
FIGURE 22b		SHEET 2 OF 2		DESIGNER JMA		
		DRAWN BY SPF		FILETIME 07 49 05		
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Figure 22b: Receiver Card Schematic Diagram (2 of 2)



TITLE <b>1PPR RECEIVER CARD SCHEMATIC          DIAGRAM (1 OF 2)</b>		FILENAME BLANK PLT		<b>UDRI</b> University of Dayton Research Institute <small>Electronic &amp; Computer Development Laboratory</small>
FIGURE 23a	SHEET 1 OF 2	DESIGNED BY JMA	DRAWN BY JHE	
© Copyright 1989, University of Dayton Research Institute E&CD Laboratory				

Figure 23a: 1PPR Receiver Card Schematic Diagram (1 of 2)



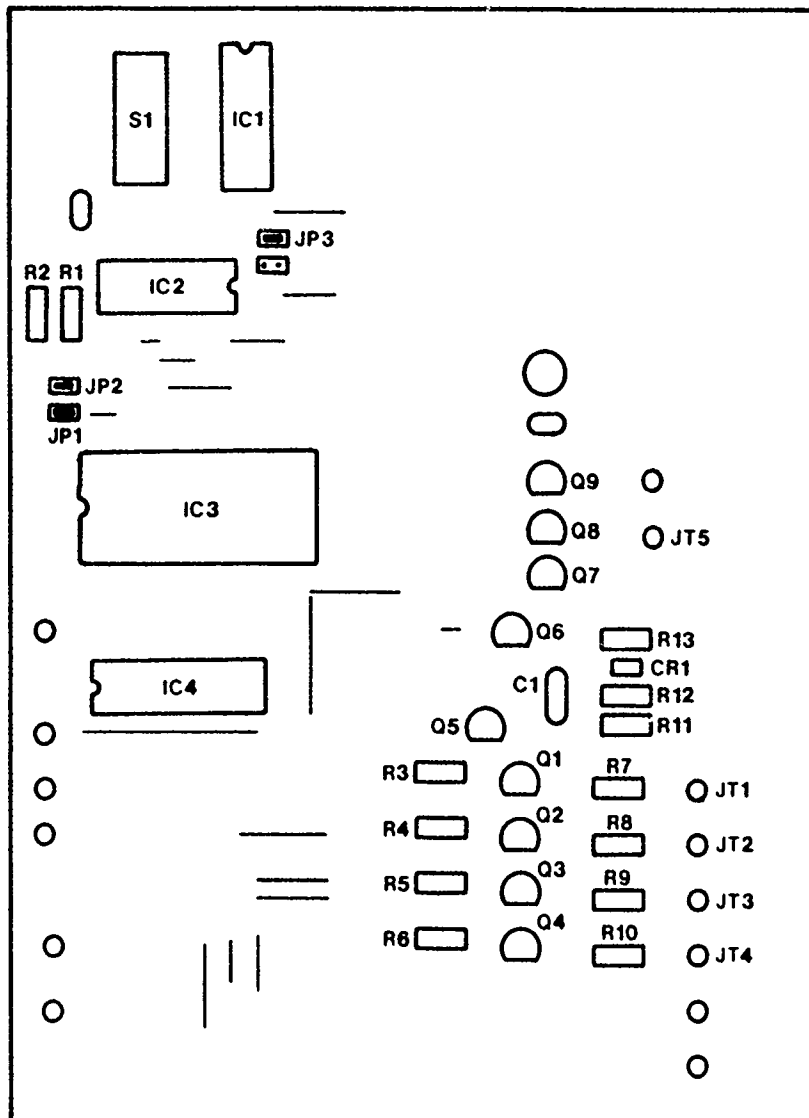
TITLE 1PPR RECEIVER CARD SCHEMATIC DIAGRAM (2 OF 2)				FILENAME BLANK PLT		<div>UDRI</div> <div>University of Dayton Research Institute</div> <div>Electronic &amp; Computer Development Laboratory</div>
				FILEDATE 07-Jul-1989		
FIGURE 23b		DESIGNER JMA		FILETIME 07 49 06		
SHEET 2 of 2		DRAWN BY SPF				
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Figure 23b: 1PPR Receiver Card Schematic Diagram (2 of 2)

# Receiver and 1PPR Receiver Cards Parts List

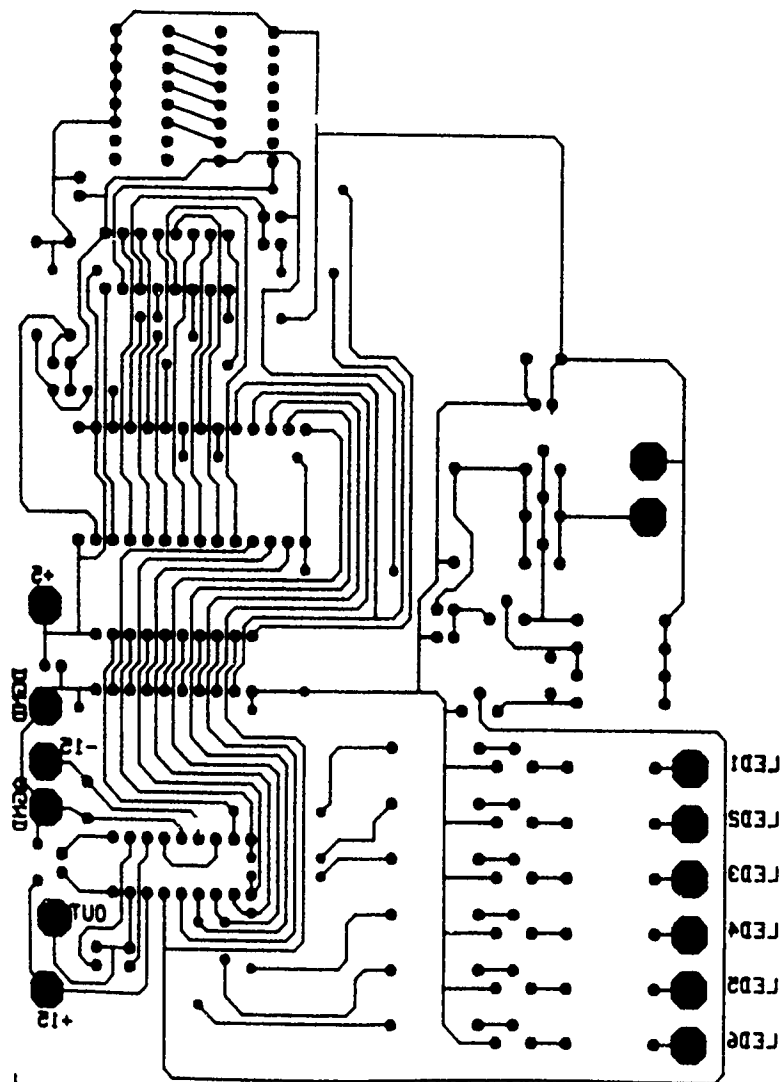
Part Number	Description
R1 - R21	100 Ohm
R22	1 KOhm
IC1 - IC6	Am26LS32
IC7	Am26LS31
J2	Ansley Blue Macs 50 pin male
J3	Ansley 64 Pin DIN VME

Table 4: Receiver and 1PPR Receiver Cards Parts List



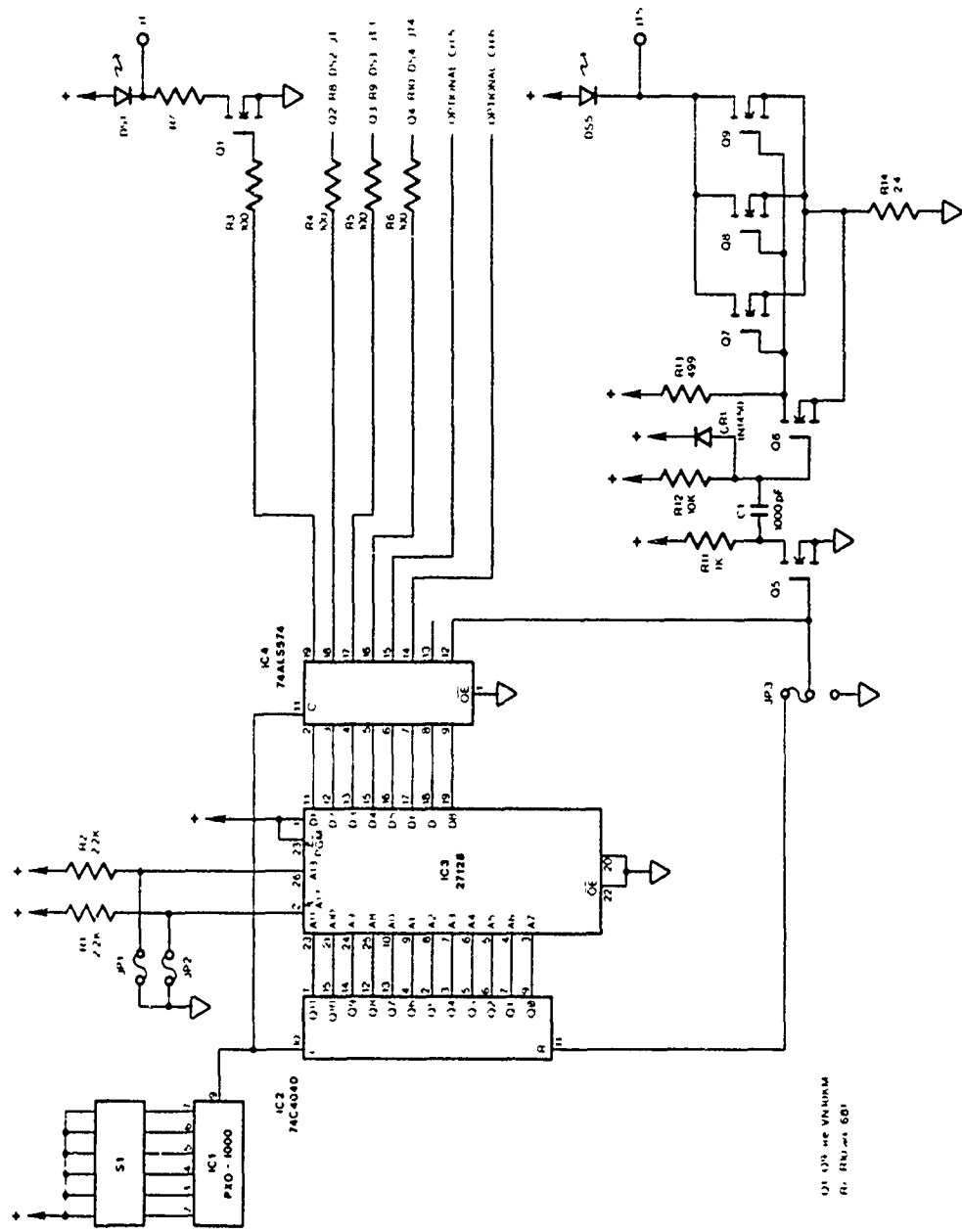
TITLE SIMULATOR BOARD COMPONENT LAYOUT				FILENAME BLANK PLT		<div>UDRI</div> <div>University of Dayton Research Institute</div> <div>Electronic &amp; Computer Development Laboratory</div>
FIGURE 24				FILEDATE 07-Jul-1989		
SHEET 1 of 1				FILETIME 07 49 06		
DESIGNER JMA				DRAWN BY SPF		
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Figure 24: Simulator Board Component Layout



TITLE <b>SIMULATOR BOARD ARTWORK</b>				FILENAME BLANK.PLT		<b>UDRI</b> University of Dayton Research Institute <small>Electronic Systems Development Laboratory</small>
FIGURE 25		DESIGNER JMA		FILEDATE 01 Jul 1989		
SHEET 1 of 1		DRAWN BY		PLOTTIME 07:19:00		
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Figure 25: Simulator Board Artwork



IC1: P10-1000  
IC2: 74C4040  
IC3: 27128  
IC4: 74ALS574

Figure 26: Simulator Board Schematic Diagram

SIMULATOR BOARD SCHEMATIC DIAGRAM				UDRI- University of Dayton Research Institute Electronic Computer Simulation Laboratory	
FILENAME		BLANK PLT			
FIGURE		07-JUL-1989			
DESIGNER		JMA		FILETIME	
DRAWN BY		SPF		07 49 06	
FIGURE 26		SHEET 1 of 1		© Copyright 1989, University of Dayton Research Institute, ESCD Laboratory	

# Simulator Board Parts List

Part Number	Description
R1, R2	2.2 KOhm
R3 - R6	100 Ohm
R7 - R10	681 Ohm
R11	1 KOhm
R12	10 KOhm
R13	499 Ohm
R14	2.4 Ohm
C1	1000 pF
IC1	PX0-1000
IC2	74C4040
IC3	27128
IC4	74ALS574
Q1 - Q9	VN10KM
DS1 - DS5	LED
CR1	1N4150

Table 5: Simulator Board Parts List

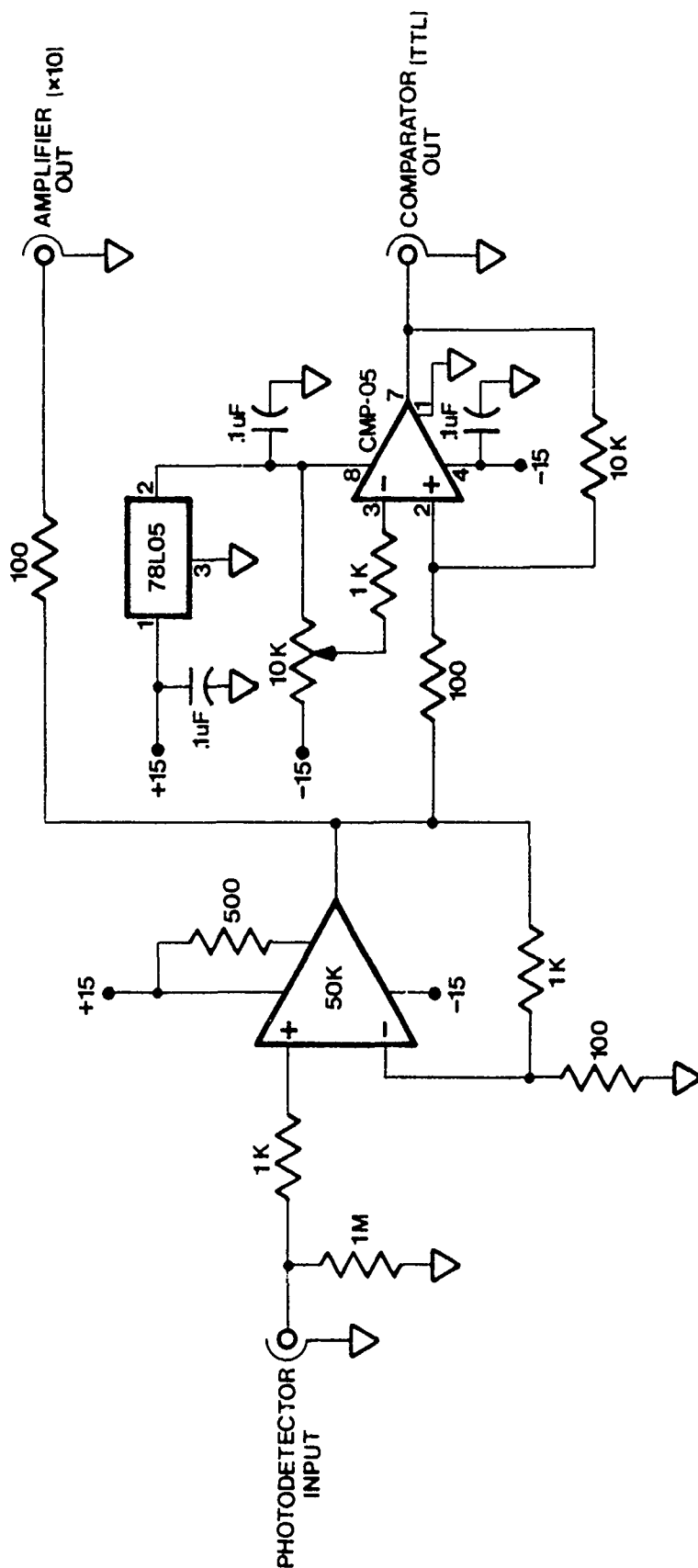


Figure 27: 1PPR Amplifier Schematic Diagram

TITLE		1PPR AMPLIFIER SCHEMATIC DIAGRAM		FILENAME		BLANK PLT		—UDRI—	
FIGURE		27		DESIGNER		07-JUL-1989		University of Dayton Research Institute	
SHEET 1 of 1		VIA		DRAWN BY		07 19 06		ELECTRONIC SYSTEMS	
© Copyright 1989		University of Dayton Research Institute		ECCO		L600-810-1			

TURBINE BLADE BACKPLANE

FRONT		CLOCK	CHAN 1	CHAN 2	CHAN 3	CHAN 4
1	INPUT	PHOTODIODE	PMT 1	PMT 2	PMT 3	PMT 4
2	ANA2	ANA GND	ANA GND	ANA GND	ANA GND	ANA GND
3	ANA3					
4	ANA4					
5	ANA GND	ANA GND	ANA GND	ANA GND	ANA GND	ANA GND
6	+15V	+15V	+15V	+15V	+15V	+15V
7	-15V	-15V	-15V	-15V	-15V	-15V
8	COMP EN	COMP EN	COMP EN	COMP EN	COMP EN	COMP EN
9	LATCH EN	LATCH EN	LATCH EN	LATCH EN	LATCH EN	LATCH EN
10	ERROR RESET	E RESET	E RESET	E RESET	E RESET	E RESET
11	ERROR	ERROR	ERROR	ERROR	ERROR	ERROR
12	DIG GND	DIG GND	DIG GND	DIG GND	DIG GND	DIG GND
13	+5V	+5V	+5V	+5V	+5V	+5V
14	CNT LATCH	CNT LATCH	CNT LATCH	CNT LATCH	CNT LATCH	CNT LATCH
15	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK
16	CLOCK/	CLOCK/	CLOCK/	CLOCK/	CLOCK/	CLOCK/
17	C23	COUNTER BIT 23	C23	C23	C23	C23
18	C22	COUNTER BIT 22	C22	C22	C22	C22
19	C21	COUNTER BIT 21	C21	C21	C21	C21
20	C20	COUNTER BIT 20	C20	C20	C20	C20
21	C19	COUNTER BIT 19	C19	C19	C19	C19
22	C18	COUNTER BIT 18	C18	C18	C18	C18
23	C17	COUNTER BIT 17	C17	C17	C17	C17
24	C16	COUNTER BIT 16	C16	C16	C16	C16
25	C15	COUNTER BIT 15	C15	C15	C15	C15
26	C14	COUNTER BIT 14	C14	C14	C14	C14
27	C13	COUNTER BIT 13	C13	C13	C13	C13
28	C12	COUNTER BIT 12	C12	C12	C12	C12
29	C11	COUNTER BIT 11	C11	C11	C11	C11
30	C10	COUNTER BIT 10	C10	C10	C10	C10
31	C9	COUNTER BIT 9	C9	C9	C9	C9
32	C8	COUNTER BIT 8	C8	C8	C8	C8
33	C7	COUNTER BIT 7	C7	C7	C7	C7
34	C6	COUNTER BIT 6	C6	C6	C6	C6
35	C5	COUNTER BIT 5	C5	C5	C5	C5
36	C4	COUNTER BIT 4	C4	C4	C4	C4
37	C3	COUNTER BIT 3	C3	C3	C3	C3
38	C2	COUNTER BIT 2	C2	C2	C2	C2
39	C1	COUNTER BIT 1	C1	C1	C1	C1
40	C0	COUNTER BIT 0	C0	C0	C0	C0

Table 6: Detector/Electronics Chassis Backplane Pinout

# Simulator Connector Pinout

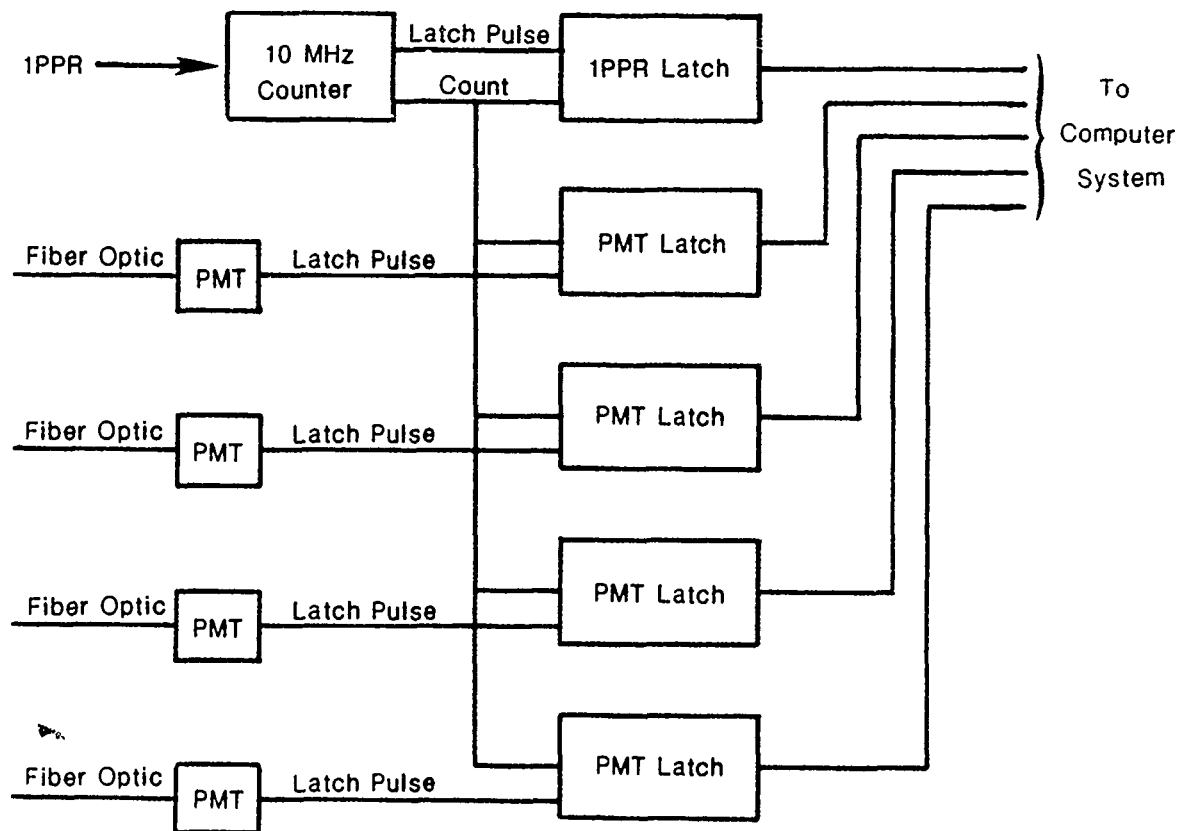
A	LED 1
B	LED 2
C	NC
D	LED 4
E	GND
F	1PPR LED
G	NC
H	GND
I	NC
J	GND
K	GND
L	NC
M	GND
N	LED 3

Table 7: Simulator Connector Pinout

# RS-232 Connector Pinouts

1	Shield
2	Transmit
3	Receive
4	NC
5	NC
6	NC
7	Signal Ground
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC

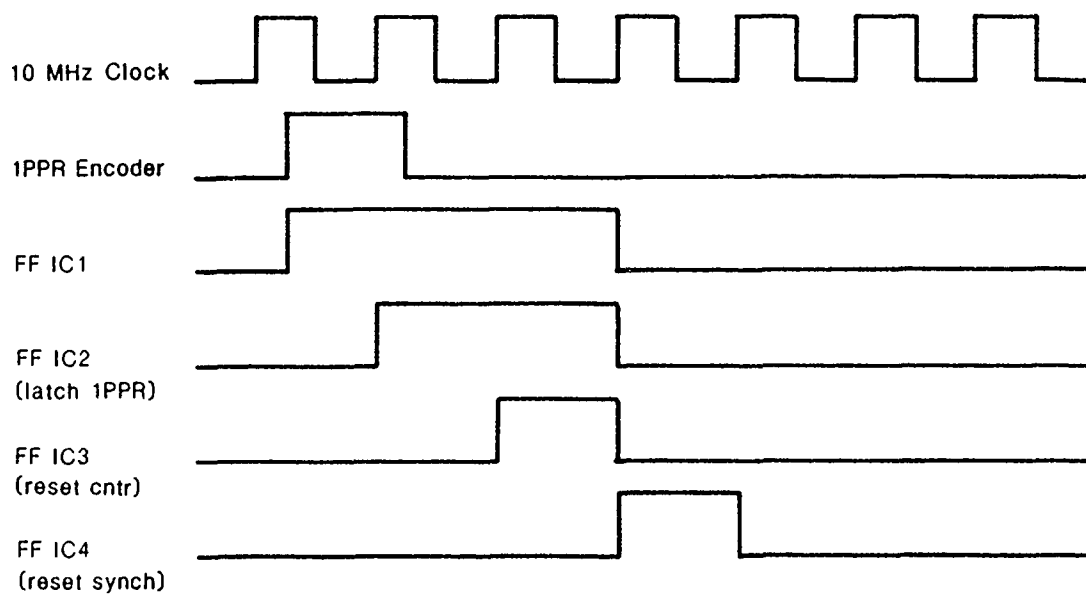
Table 8: RS-232 Connection Pinouts



TITLE <b>DETECTOR/ELECTRONICS CHASSIS          BLOCK DIAGRAM</b>				FILENAME BLANK PLT	
				FILEDATE 07-Jul-1989	
FIGURE 28	SHEET 1 of 1	DESIGNER ECD	DRAWN BY MJG	FILETIME 07 49 06	
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Electronic & Computer Development Laboratory

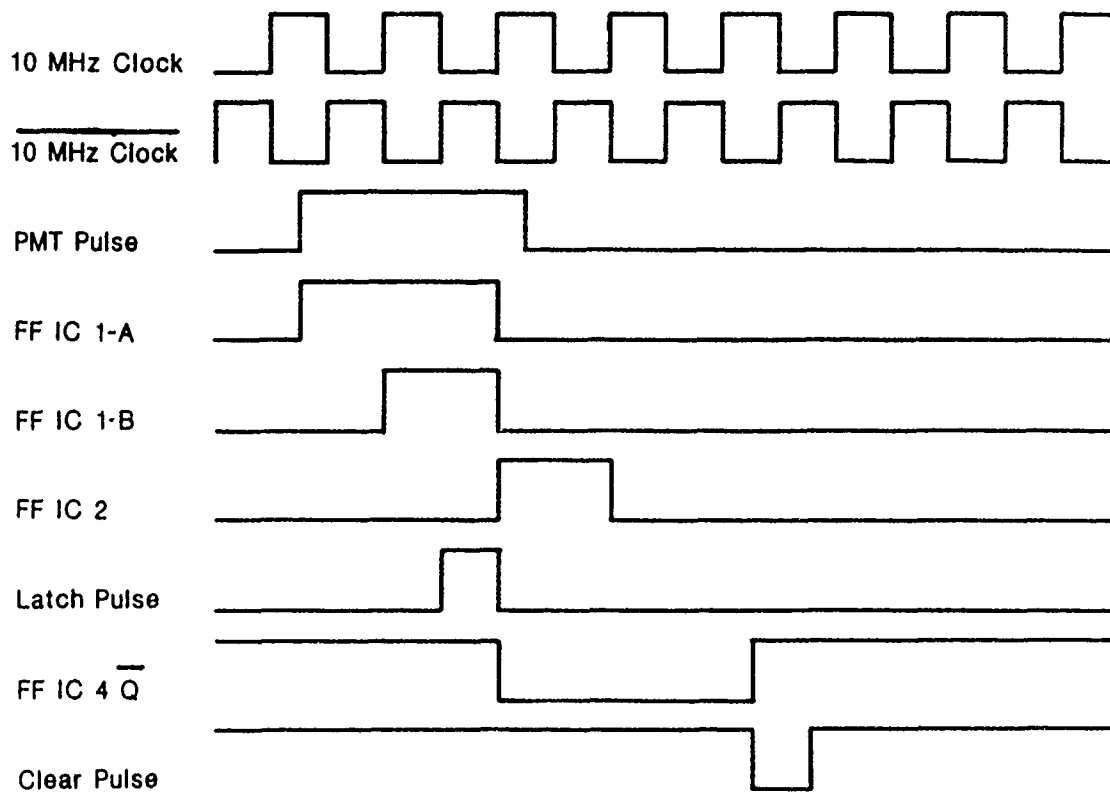
Figure 28: Detector/Electronics Chassis Block Diagram



<b>TITLE</b> COUNTER SYNCHRONIZATION TIMING DIAGRAM				<b>FILENAME</b> BLANK PLT	
<b>FIGURE</b> 29				<b>FILEDATE</b> 07-Jul-1989	
<b>SHEET</b> 1 of 1		<b>DESIGNER</b>		<b>DRAWN BY</b> MJG	
<b>FIGURE</b> 29				<b>FILETIME</b> 07 49 05	
© Copyright 1989, University of Dayton Research Institute E&CD Laboratory					

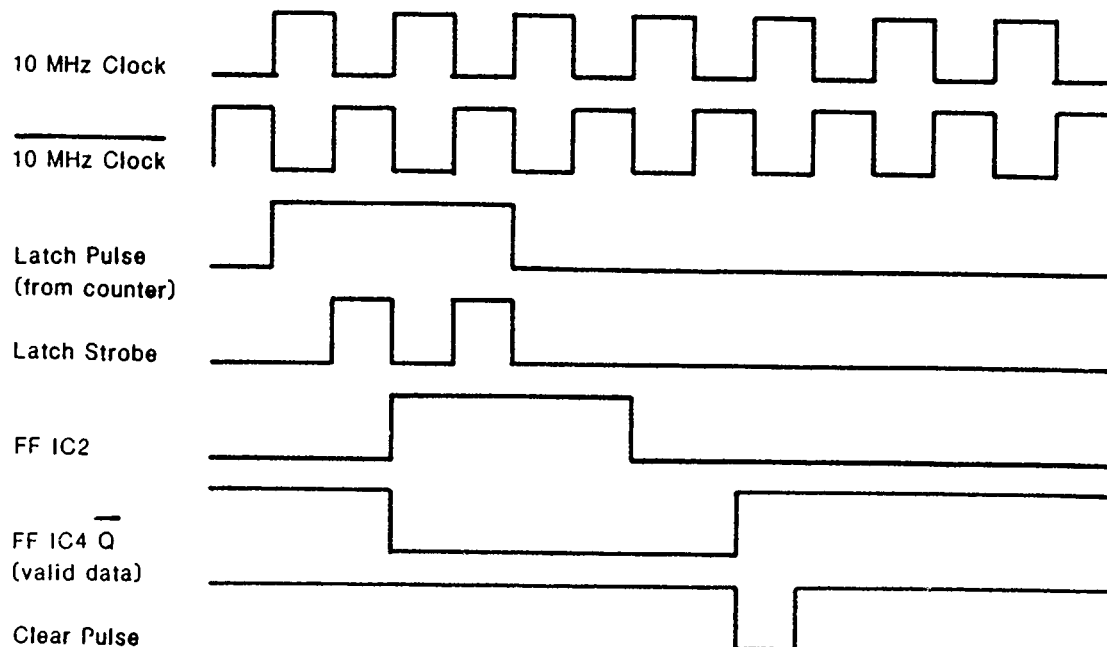
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 Research Institute  
 Electronic & Computer Development Laboratory

Figure 29: Counter Synchronization Timing Diagram



TITLE LATCH CARD TIMING DIAGRAM				FILENAME BLANK PLT		<b>UDRI</b> University of Dayton Research Institute <small>Electronic &amp; Computer Development Laboratory</small>
				FILEDATE 07-Jul-1989		
FIGURE 30	SHEET 1 of 1	DESIGNER	DRAWN BY MJG	FILETIME 07 49 06		
© Copyright 1989, University of Dayton Research Institute ESCO Laboratory						

Figure 30: Latch Card Timing Diagram



TITLE 1PPR LATCH CARD TIMING DIAGRAM				FILENAME BLANK PLT	<b>UDRI</b> University of Dayton Research Institute <small>Electronic &amp; Computer Development Laboratory</small>
				FILEDATE 07-Jul-1989	
FIGURE 31	SHEET 1 of 1	DESIGNER	DRAWN BY MJG	FILETIME 07-19-06	

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Figure 31: 1PPR Latch Card Timing Diagram

# NSMS Data Acquisition System - Tape Format

Fixed length - 512 byte records

block 0

bytes 0.. 3 : nb = number of blades  
 bytes 4.. 7 : nr = number of revolutions  
 bytes 8.. 11 : ns = number of stations  
 bytes 12.. 15 : average speed  
 bytes 16.. 19 : minimum speed  
 bytes 20.. 23 : maximum speed  
 bytes 24..127 : unused  
 bytes 128..136 : run date (DD-MMM-YY)  
 bytes 137..141 : excitation frequency  
 bytes 142..149 : run time (HH:MM:SS)  
 bytes 150..165 : radius  
 bytes 166..245 : run description  
 bytes 246..261 : run id  
 bytes 262..421 : specimen description  
 bytes 422..437 : specimen id  
 bytes 438..511 : unused

nbrd = number blocks for rev data =  $\text{int}((nr + 127)/128)$   
 nbdd = number blocks for blade data =  $\text{int}((nr*nb+127)/128)$

block 1..nbrd

bytes 0..3 : rev 1 time for station 1  
 bytes 4..7 : rev 2 time for station 1  
 .  
 .

block nbrd+1..nbrd+nbdd

bytes 0..3 : rev 1 blade 1 time for station 1  
 bytes 4..7 : rev 1 blade 2 time for station 1  
 .  
 .  
 bytes nb\*4-4..nb\*4-1 : rev 1 blade nb time for station 1 bytes nb\*4..nb\*4+1 : rev 2 blade 1 time for station 1 .  
 .

repeat from block 1 for station 2, 3 and 4

tape mark

Table 9: Magnetic Tape Record Format